Microelectronics Packaging at APL: Delivering Custom Devices for Critical Missions

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ABSTRACT

At the Johns Hopkins University Applied Physics Laboratory (APL), microelectronics packaging includes a wide range of microelectronics fabrication and assembly technologies. Conventional microelectronics packaging integrates electronics on a bare die level. At APL, microelectronics packaging has evolved to include packaging of customized miniature electrical, mechanical, and electromechanical devices. APL's engineers design, fabricate, assemble, inspect, screen, repair, and provide depackaging solutions for diverse projects and sponsors. Because of its technological capabilities and facilities, along with the skill sets of its staff members, APL is able to prototype and produce a broad range of devices, such as sensors, detectors, and communications and computing hardware, for mission-critical projects supporting research and development, defense, near-Earth and deep-space missions, and medicine. This article highlights microelectronics packaging capabilities at APL.

INTRODUCTION

Conventional electronics packaging begins with nanofabrication or microfabrication, where electronic circuits or electromechanical features are fabricated into wafers in the nanometer or micrometer scale. (Refer to the article by Currano et al.[1] for more on nanofabrication at APL.) These wafers are singulated into chips that then get assembled into single-chip or multi-chip microelectronics devices—this chip-level integration is the traditional scope of microelectronics packaging. These devices are then mounted onto boards or systems that get installed into enclosures.

Most devices packaged in APL's microelectronics cleanroom labs are high-reliability monolithic and hybrid microelectronic packages that require compliance with military and industry specifications and standards, such as MIL-PRF-38534,[2] MIL-PRF-38535,[3] MIL-STD-883,[4] NASA standards, IPC J standards, or similar. Consequently, APL teams have developed and established processes to comply with the Lab's quality management system or with industry standards, such as AS9100.[5] Commercial-class single-chip and multi-chip modules with newer substrate types, such as chip-on-laminate, comprise the second largest portion of microelectronic

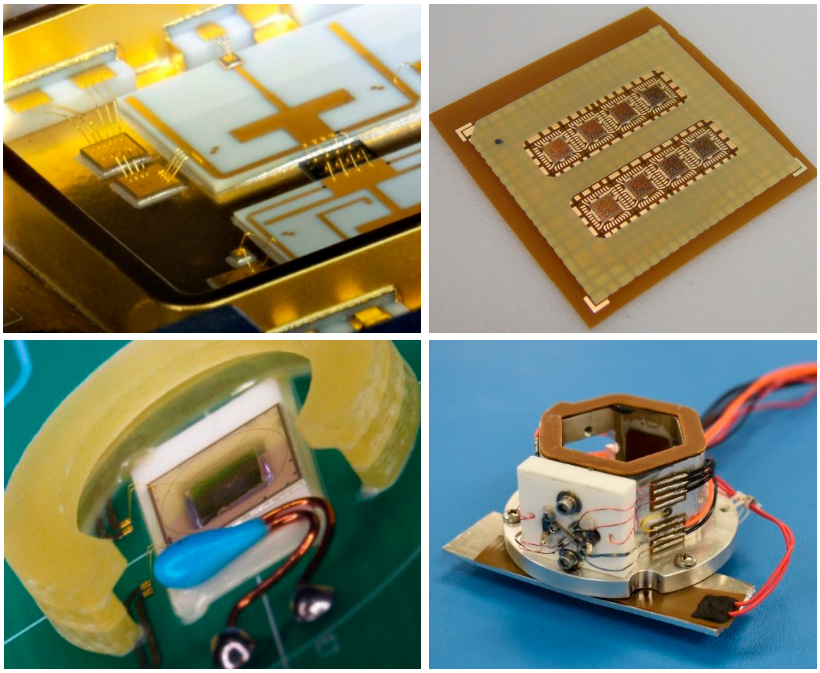

Figure 1. Diverse devices packaged at APL. Top left, a high-reliability hybrid microelectronics package assembled to comply with MIL-STD-883 Class H requirements.[6] Top right, silicon chips epoxy-attached to an eight-up laminate panel, then wire bonded with a 25-µm-diameter gold wire. The wire bonded chips were encapsulated and then singulated onto quad flat no-lead packages (QFNs). Bottom left, a thermistor soldered onto a printed circuit board (PCB). A die was mounted on laser-cut ceramic pieces using an optical adhesive. The stacked FR4 pieces serve as mechanical protection for gold ball wire bonds from die to PCB. This work was supported by the NASA Maturation of Instruments for Solar System Exploration (MatISSE) program under grant agreement 80NSSC17K0599 issued through the Science Mission Directorate. Bottom right, packaging of a miniature electromechanical device.

devices packaged at APL. The rest are a broad spectrum of prototypes and flight builds of custom miniaturized electromechanical hardware. Figure 1 shows a variety of devices packaged at APL.

APL staff members use many processing techniques (Table 1) to package these various kinds of devices in support of critical missions across the Lab. Because APL's microelectronics packaging teams are tasked with delivering highly customized devices, they do not always pursue industry trends geared toward commercial applications. Many of APL's packaging processes and applications are described in more detail in the sections that follow. APL's microelectronics packaging lab distinguishes itself from commercially available alternatives by supporting a very highly customized, low-volume mixture of prototype builds and high-reliability devices that are not designed to be scaled up for mass production—for instance, hardware for one spacecraft designed to crash into a celestial object and another designed to study the surface of Saturn's largest moon.

Table 1. Microelectronics packaging processes at APL

Fundamental Microelectronics Processes	Fabrication and Depackaging Processes
Eutectic die bonding	Decapsulation and depackaging
Thermocompression bonding	Extracted die plating
Epoxy bonding	Lapping and polishing
Wire bonding	Back-side processing
Underfill and encapsulation	Micromilling
Hermetic sealing	Laser cutting
Soldering	Chemical milling
Dicing	

APL'S MICROELECTRONICS PACKAGING FACILITY

Microelectronics packaging processes are performed in environment-controlled ISO Class 7[7] (FED-STD-209E Class 10,000[8]) cleanrooms in APL's microelectronics packaging lab. These rooms have hard-sided walls and high-efficiency particulate air (HEPA) filtration systems to ensure that air cleanliness levels do not exceed 10,000 particles (≥0.5 µm) per cubic foot. All workstations are configured to prevent and control electrostatic discharge.

The cleanrooms are outfitted with essential microelectronics assembly equipment enabling staff members to perform the various microelectronics packaging processes summarized below. An assortment of high-magnification and high-power microscopes are available to support visual inspections in the nanometer and micrometer scale. Wire pull and die shear testers are available to perform MIL-STD-883-compliant destruct and non-destruct tests. In addition, MIL-STD-compliant screening equipment is available in APL cleanrooms for performing fine and gross leak tests, temperature cycling, constant acceleration, particle impact noise detection (PIND) tests, and temperature and humidity tests.

MICROELECTRONICS PACKAGING, FABRICATION, AND DEPACKAGING PROCESSES AT APL

As mentioned, APL teams package a wide variety of devices using many processing techniques. These techniques include fundamental microelectronics processes, such as bonding, underfilling and encapsulation, hermetic sealing, soldering, screening, and dicing. APL staff

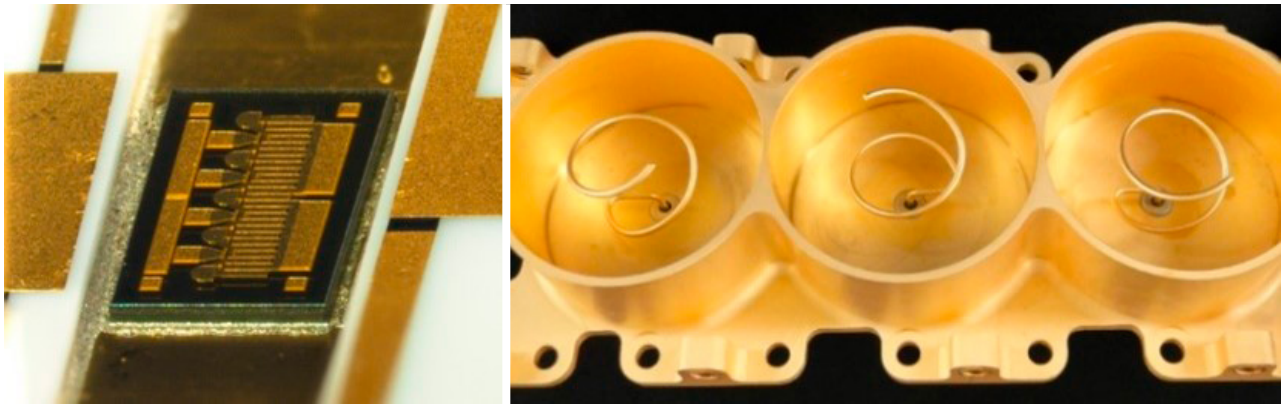

Figure 2. Eutectic die bonding examples. Left, a GaAs die eutectically mounted to a gold-plated copper-molybdenum-copper package using 80Au/20Sn solder preform for the IMAP mission. Right, hermetic feedthroughs eutectically mounted to gold-plated aluminum housing using 80Au/20Sn solder preform for the Europa Clipper fan beam antenna.

members also apply fabrication and depackaging techniques, such as decapsulation, die extraction and plating, lapping and polishing, micromilling, laser cutting, and chemical milling.

Eutectic die bonding using a solder preform, such as gold-tin, is the quintessential die mounting technique for attaching die elements, such as gallium arsenide (GaAs) and gallium nitride (GaN), to high-reliability hybrid microelectronics devices. Gold-tin eutectic solder, such as 80Au/20Sn, melts at 280°C and is typically used with a forming gas instead of flux. This eutectic die bonding technique is not limited to hybrid packages; it can also be used to attach components that require high-reliability seals, such as hermetic feedthroughs. Recent APL applications, shown in Figure 2, include packages for the Interstellar Mapping and Acceleration Probe (IMAP)[9] and Europa Clipper[10,11] missions.

Thermocompression bonding metallurgically bonds two metal surfaces by applying accurately controlled heat and bonding force onto mating components. An example application is thermocompression bonding a bottom termination leadless component onto a silicon chip with gold stud bumps acting as interconnects. The process temperature ranges from 300°C to 350°C for gold-to-gold interconnect.

Epoxy bonding is the most prevalent method of attaching components in microelectronics packages. The epoxy used varies depending on the device's integration requirements. Figure 3 shows an electrically and thermally conductive silver-filled epoxy used to attach a substrate onto a package. A nonconductive epoxy bonds glass onto a plastic housing, while a combination of conductive and nonconductive epoxies assembles an electromechanical device. Low-outgassing organic-based epoxies and optical adhesives are some other examples. Cure times vary depending on the bond line thicknesses and materials.

Wire bonding remains the most reliable, straightforward, and widely used interconnection method in many microelectronics packages. APL has a variety of manual

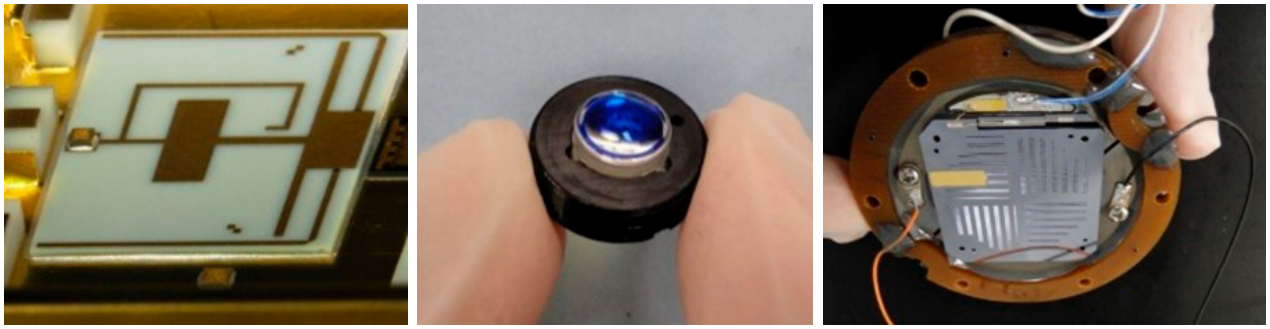

Figure 3. Epoxy bonding examples. Left, a hybrid package for the IMAP mission where a 0.005-in.-thick alumina substrate is epoxy-attached to a housing using a silver-filled conductive epoxy. A 0.015-in. square capacitor was epoxy-attached to a pad on the substrate. The attachments on this device must meet the MIL-STD-883 Test Method 2017 Class H requirements. Center, a glass bonded onto a plastic housing using a nonconductive epoxy that cures at room temperature. Right, a three-layer stack of etched silicon substrates bonded with nonconductive epoxy onto a titanium plate. Ribbon wires bonded with silver-filled conductive epoxy connect the stacked silicon layers to external terminals.

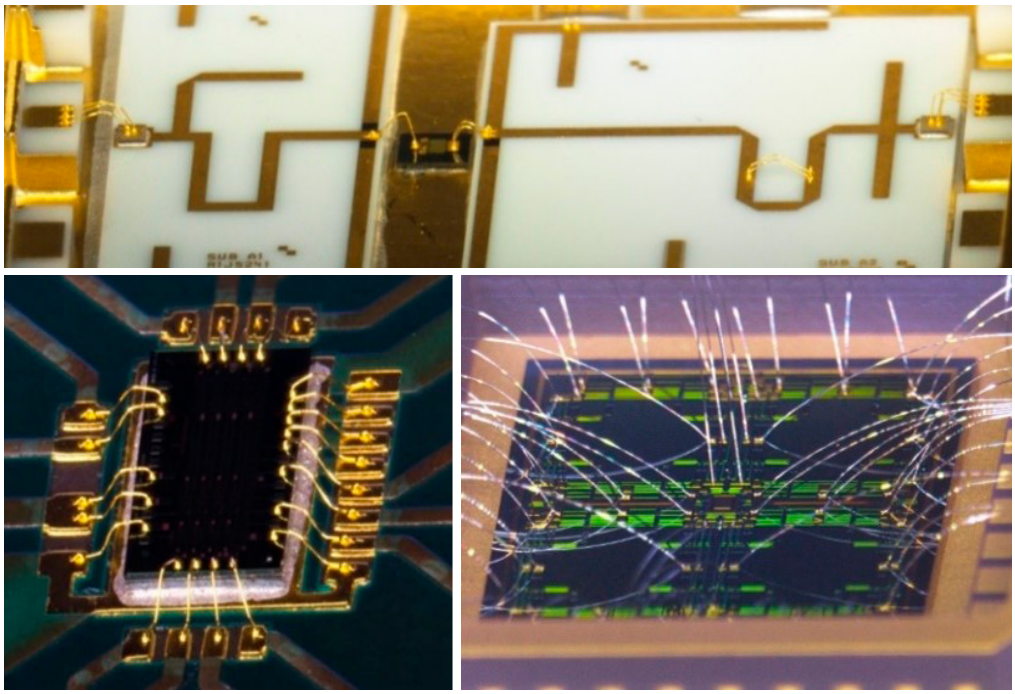

Figure 4. Top, gold ball wire bonding constant-length wires on an RF package. Bottom left, gold ball bonding a silicon chip on an organic substrate, a PCB. Bottom right, aluminum wedge bonding a microelectromechanical systems device on a leadless chip carrier (the package was wire bonded for the Army Research Laboratory).

and automated wire bonders for gold ball wire bonding, aluminum wedge bonding, and copper wire bonding. As expected, wire diameters have gotten smaller to adapt to smaller die bond pads and finer pitch. Gold wires as small as 12.5 µm in diameter have been used on die bond pads as small as 35 × 70 µm with pad pitch of 40 µm. Not only are wires getting smaller, but bond pad metallization also changes from traditional gold or aluminum pads to newer materials, such as niobium titanium nitride (NbTiN) thin films on silicon substrate. Wire bonding can be integrated into many applications, such as gold ball bonding constant-length wires on a radio frequency (RF) package, gold ball bonding a chip on organic substrate, and aluminum wedge bonding a microelectromechanical systems device on a leadless chip carrier (Figure 4).

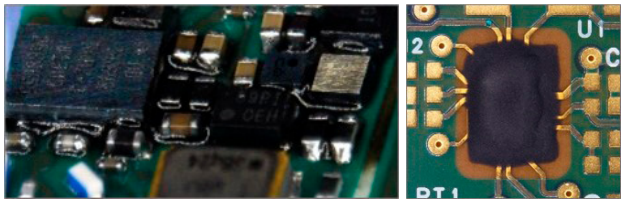

Figure 5. Left, an underfill material covering the solder joints of the components soldered onto the PCB. Right, an encapsulation material fully covers the die and all the wire bonds that connect it to the PCB.

The main objective of ***underfill*** and/or ***encapsulation*** is to protect interconnects or joints from damage during subsequent assembly processes or in the field. Underfill and encapsulation materials shown in Figure 5 are polymer materials dispensed onto specific locations of the circuit.

Hermetic sealing (Figure 6), also called seam sealing or seam welding, is typically performed on high-reliability microelectronics packages to create an airtight seal so the devices can survive harsh conditions in space, deep below Earth's surface, or in other extreme environments. APL has a seam welder to join similar or dissimilar materials along a continuous seam.

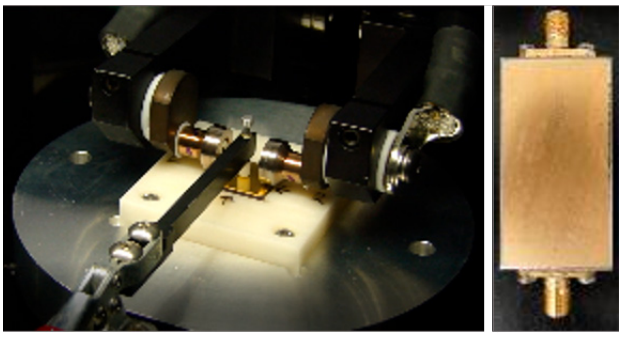

Figure 6. Hermetic sealing using special electrodes that weld the lid onto the package to create a continuous seam. This type of sealing is typically performed on high-reliability microelectronics packages that need to survive in harsh conditions.

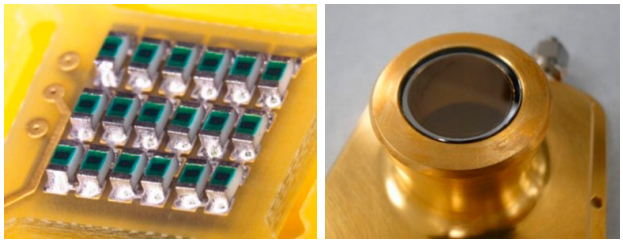

Figure 7. Soldering examples. Left, rows of 0402 chip resistors soldered onto FR4 board with 63Sn/37Pb solder paste, which melts at 183°C, and reflowed at peak temperature of ~220°C. Right, a glass window soldered onto a gold-plated aluminum housing using an In/Pb/Ag solder ribbon to form a vacuum seal.

Soldering is used on devices, like the one shown in Figure 7, that need solderable components mounted or wires soldered onto them using solder alloys, such as eutectic tin-lead 63Sn/37Pb with a melting point at 183°C or the lead-free alloy Sn/Ag/Cu with a melting point at 217°C. Soldering also applies to nonelectronic devices using alternative solder alloys, such as In/Pb/Ag with a melting point at 153°C. Soldering typically uses flux that is compatible with the materials and alloys to solder.

Dicing custom-made packages, like the one shown in Figure 8, was one of the enabling technologies for developing smaller and thinner QFNs. APL has the capability to dice many materials, from standard microelectronic materials to materials such as PCBs and metals.

Decapsulation is the process of removing packaging material from the front side of a packaged part to reveal the integrated circuit (IC) surface. The process uses a combination of sulfuric and nitric acids. Decapsulation does not damage package leads or wire bonds. The process allows the IC to be tested and evaluated in its original package. **Depackaging** is a destructive process by which the IC is completely removed from its original package to be evaluated. With the IC removed from its original package, it can be assembled into a new package.

Extracted die plating allows the reuse of die, like the one shown in Figure 9, that have been depackaged

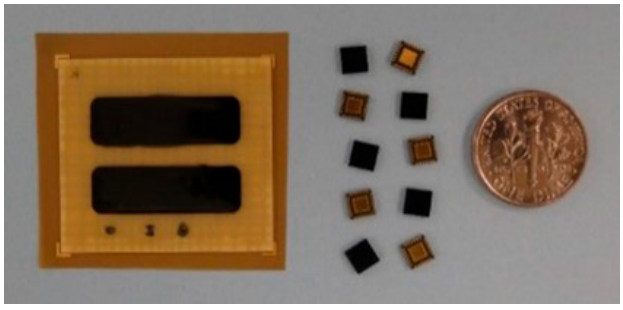

Figure 8. Dicing a custom-made package into QFNs. APL can dice many materials, from standard microelectronic materials to materials such as PCBs and metals.

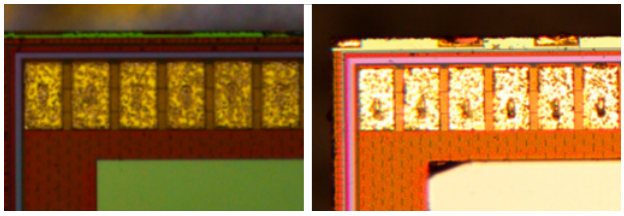

Figure 9. Replating of extracted die. With extracted die plating, pads become once again wire bondable with good adhesion, allowing depackaged die to be reused.

from a package or board. With this plating process, pads become once again wire bondable with good adhesion.

Lapping and polishing (Figure 10) is used when bulk material needs to be thinned or polished to a mirror-like state. This process has enabled significant reduction in the QFN footprint. APL can make a QFN just larger than the die itself and has used lapping and polishing to thin stacked die to as thin as ~50 µm.

A small milling bit ranging in diameter from 3 to 0.4 mm is used to create cavities in package material. The milling bit can also be used remove package lids without damaging the package.

Laser cutting (Figure 11) is the process of cutting features through materials, like ceramic plate, aluminum sheets, laminate materials, and flexible substrates, such as Kapton. Laser cutting is useful for cutting oddly shaped or custom-shaped features.

Chemical milling etches out or mills parts, such as the beryllium copper sheet shown in Figure 12, that

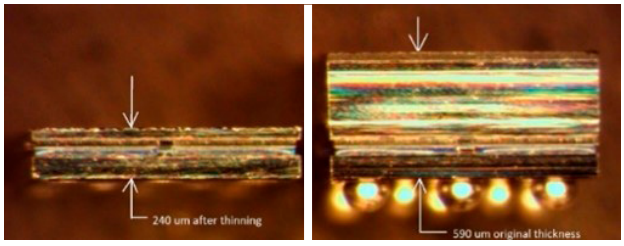

Figure 10. Lapping and polishing to thin die. Left, side view of a commercial die after it is thinned. Right, original die thickness. APL has used lapping and polishing to thin stacked die to as thin as ~50 µm.

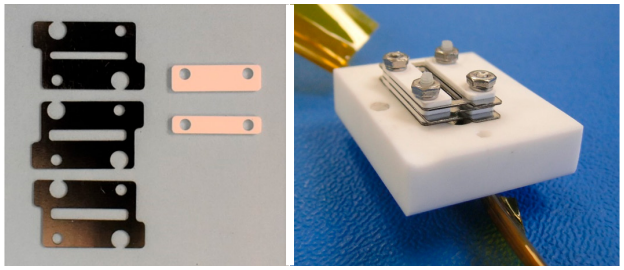

Figure 11. Laser cutting. Molybdenum sheets and alumina laser-cut and stacked onto an electromechanical device.

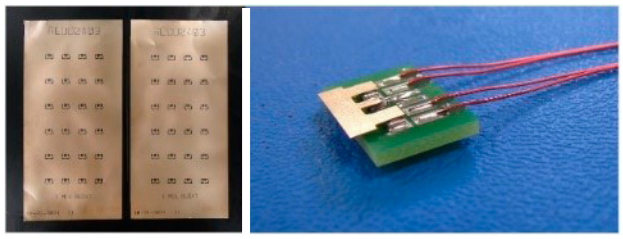

Figure 12. Chemical milling. A singulated chemically milled 0.005-in.-thick beryllium copper is bonded onto a PCB using a thermally conductive, electrically insulative epoxy.

are otherwise difficult or impossible to fabricate using mechanical milling or machining methods. Chemically milled parts are generally made using material thinner than 1.0 mm. APL can chemically mill parts out of copper, copper alloy, aluminum, and stainless steel.

SELECTED EXAMPLES

DART Camera

APL developed a high-resolution telescopic camera, Didymos Reconnaissance and Asteroid Camera for Optical Navigation (DRACO),[12] for the DART spacecraft[13] (Figure 13). This camera consisted of an optical imaging chip assembled on a custom PCB. The PCB and mechanical parts—heat sink, frame, and cover—were designed and fabricated at APL. The multilayer rigid-flex PCB was plated with nickel palladium and gold (ENEPIG). This special-purpose surface finish allows for both soldering surface-mount devices and wire bonding onto the PCB. The heat sink was attached to the PCB, and the imaging chip package was mounted onto the heat sink. Electrical connections to the optical chip were made using ultrasonic wedge bonding technology to attach 32-µm (0.00125 in.)-diameter aluminum wires.

DART Radial Line Slot Antenna

APL also fabricated the Radial Line Slot Antenna (RLSA)[14] for the DART spacecraft (Figure 14). The design called for a small cone-shaped radiating element to be attached to the center conductor pin of a connector to feed the microwave signal to the antenna. An important consideration for the radiator cone is that it can heat up to over 200°C during operation. Standard tin-lead alloy solders melt at these temperatures. The solution was to use a high-temperature solder, such as gold-tin, which melts around 300°C, to reflow attach the cone. In addition, the insulation and center pin lengths of the original connector were modified to dimensions specified by the design engineer. The small cone was machined in APL's machine shop and gold-plated in the

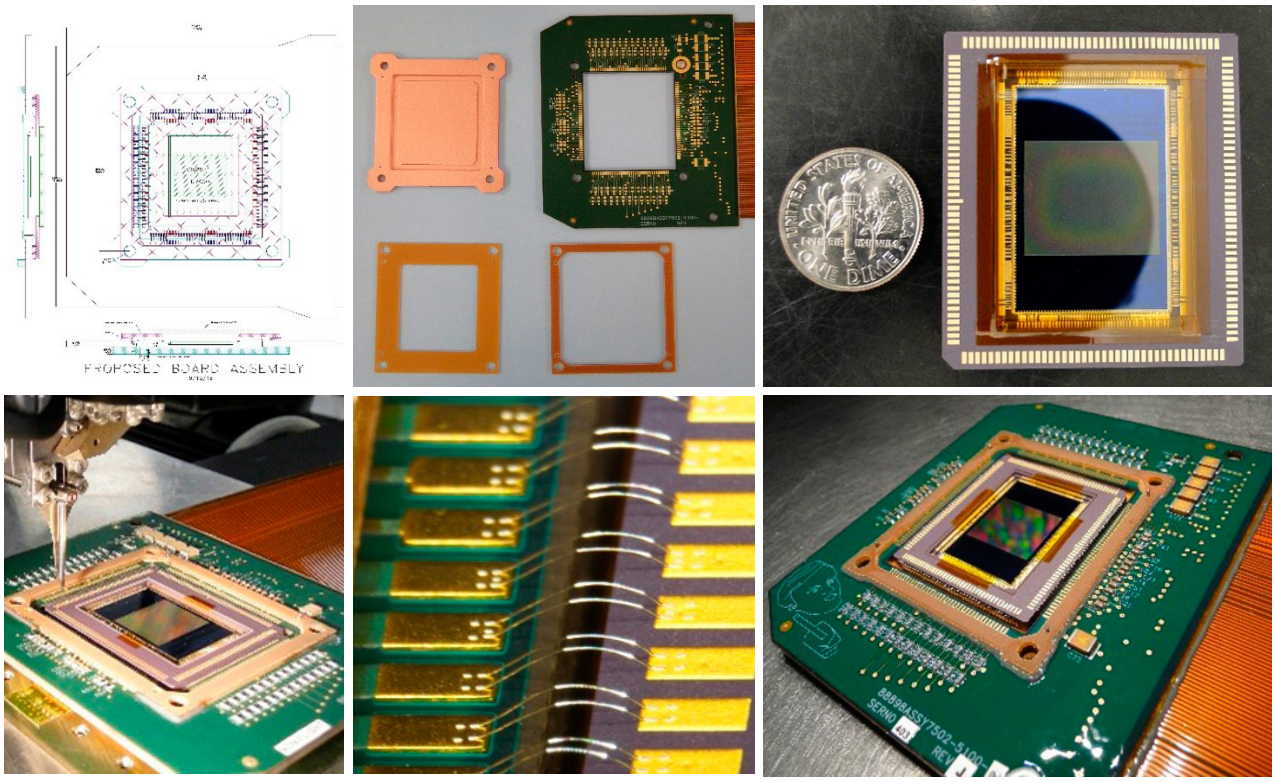

Figure 13. Microelectronics assembly of the micro-imager chip for DRACO, a high-resolution telescopic camera for the DART mission. The micro-imager chip is wire bonded to the circuit board. This design was a joint effort by engineers in APL's microelectronics area and its Space Exploration Sector. The circuit board, heat sink, frame, and cover are also shown.

Figure 14. RLSA for the DART mission. The radiator cone can heat up to over 200°C during operation, requiring a high-temperature solder to reflow attach the cone. In addition, the insulation and center pin lengths of the original connector were modified. The small cone was machined in APL's machine shop and gold-plated in the microelectronics fabrication lab. Special mechanical fixtures were also made to facilitate the modification and solder reflow attachment of the cone to the center pin.

microelectronics fabrication lab. Special mechanical fixtures were also made to facilitate the modification and solder reflow attachment of the cone to the center pin.

Dragonfly DragonCam Light-Emitting Diode Array

Dragonfly's[15] DragonCam light-emitting diode (LED) array (Figure 15) is designed to image Titan's surface. The LED array will illuminate sampling sites over multiple wavelengths, including ultraviolet, visible, and near infrared, using nine multispectral LEDs. The array consists of 180 individual LEDs on a multilayer PCB fabricated at APL. To keep the array small and lightweight, the board includes bare LED die spaced 2.5 mm apart. The LEDs are attached with a silver-filled conductive adhesive and electrically connected with 25-µm-diameter gold wire using a thermosonic wire bonding process.

CONCLUSION

Electronic systems continue to demand more miniaturization.[16] Devices that were traditionally designed for board-level and even system-level electronics are being miniaturized. Microelectronics packaging will always be the bridge from microfabricated chips to board-level electronics. APL has the unique combination of technological capabilities, state-of-the-art facilities, and expertise

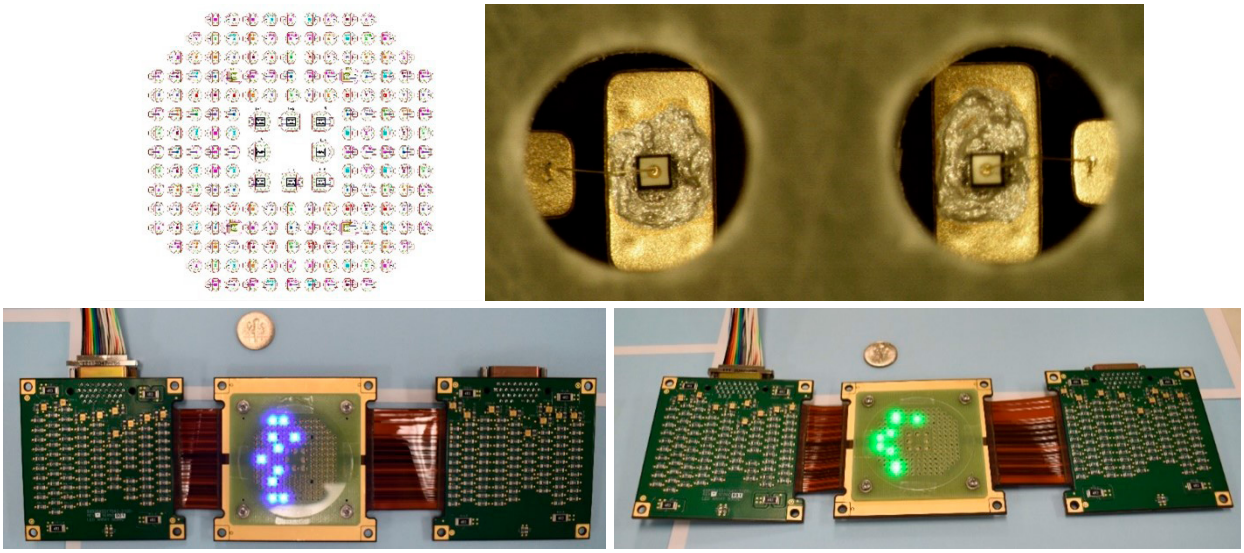

Figure 15. DragonCam LED array for the Dragonfly mission. The array, consisting of 180 individual LEDs on a multilayer PCB, was fabricated at APL. Bare LED die are spaced 2.5 mm apart and attached with a silver-filled conductive adhesive and electrically connected with 25-µm-diameter gold wire using a thermosonic wire bonding process.

to prototype and produce a broad range of devices for diverse applications in support of critical missions.

APL will continue to expand its capabilities to remain at the forefront of technological advances and to meet its sponsors' requirements. The Lab is advancing its processes and technologies to support finer-pitch wire bonding and high-accuracy flip chip bonding to enable packaging of multi-stack devices. The areas of growth are 3-D assembly and photonics packaging.

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REFERENCES

[1]L. J. Currano, L. H. Oh, C. M. Zgrabik, A. A. Podpirka, C. T. Mooers, et al., "Nanofabrication at APL: Novel techniques to deliver innovative devices," *Johns Hopkins APL Tech. Dig.*, vol. 36, no. 4, pp. 388–396, https://secwww.jhuapl.edu/techdigest/Content/techdigest/pdf/V36-N04/36-04-Currano.pdf.

[2]*Performance Specification Hybrid Microcircuits, General Specification for*, MIL-PRF-38534, Department of Defense, Washington, DC.

[3]*Performance Specification: Integrated Circuits (Microcircuits) Manufacturing, General Specification for*, MIL-PRF-38535, Department of Defense, Washington, DC.

[4]*Department of Defense Test Method Standard: Microcircuits, Test Standards*, MIL-STD-883, Department of Defense, Washington, DC.

[5]Quality Systems - Aerospace - Model for Quality Assurance in Design, Development, Production, Installation and Servicing, AS9100, SAE International, Warrendale, PA.

[6]J. R. Dennison, S. Cheng, A. Sharma, J. Lehtonen, N. Dalal, R. Wallis, and D. Matlin, "X-band GaN SSPA for near Earth and deep space missions," in *Proc. 2022 IEEE Aerosp. Conf. (AERO)*, 2022, pp. 01–09, https://doi.org/10.1109/AERO53065.2022.9843728.

[7]"ISO 14644 history and usage," IEST, https://www.iest.org/Standards-RPs/ISO-Standards/ISO-14644-Series.

[8]*Federal Standard: Airborne Particulate Cleanliness Classes in Cleanrooms and Clean Zones*, FED-STD-209E, Department of Defense, Washington, DC, 1992, http://everyspec.com/FED-STD/FED-STD-209E_21739/.

[9]"Interstellar Mapping and Acceleration Probe." Princeton University. https://imap.princeton.edu/.

[10]"Europa Clipper." NASA. https://europa.nasa.gov/.

[11]A. Sharma, C. Carpenter, J. T. Will, and J. R. Dennison, "Europa Clipper X-band antennas," in *Proc. 2022 IEEE Int. Symp. on Antennas Propag. and USNC-URSI Radio Sci. Mtg. (AP-S/URSI)*, 2022, pp. 996–997, https://doi.org/10.1109/AP-S/USNC-URSI47032.2022.9886019.

[12]D. Bekker, R. Smith and M. Q. Tran, "Guiding DART to impact—The FPGA SoC design of the DRACO image processing pipeline," in *Proc. 2021 IEEE Space Comput. Conf. (SCC)*, 2021, pp. 122–133, https://doi.org/10.1109/SCC49971.2021.00020.

[13]"Double Asteroid Redirection Test." APL. https://dart.jhuapl.edu/.

[14]M. G. Bray, "Design, development and testing of NASA's DART Radial Line Slot Array Antenna," in *Proc. Natl. Radio Sci. Mtg. (NRSM)*, 2023, paper 1156, https://www.usnc-ursi-archive.org/nrsm/2023/papers/1156.pdf.

[15]"Dragonfly." APL. https://dragonfly.jhuapl.edu/.

[16]G. V. Clatterbaugh, C. V. Banda, and S. J. Lehtonen, "Reliable miniature electronic and optical interconnects for low-volume applications," *Johns Hopkins APL Tech. Dig.*, vol. 28, no. 1, pp. 47–57, 2008, https://www.jhuapl.edu/Content/techdigest/pdf/V28-N01/28-01-Clatterbaugh.pdf.

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