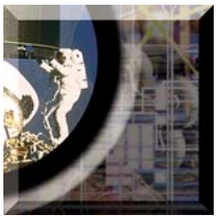

Emerging Technologies with Commercial Potential

We are embarking on the next era of spacecraft use in commercial applications, spanning telecommunications to Earth sciences. Technologies as broad ranging as new integrated digital/analog chips, miniaturization, instruments technologies, autonomy, and modeling are key to future scientific and commercial space missions.

APL's Advanced Technology Development (ATD) Program sponsored by NASA is investigating these new technologies in order to achieve significant reductions in the size and power of system components; develop numerous new technologies to make concepts such as nanosatellites, microsatellites, and satellite constellations (i.e., formation flying) viable from a mass and power standpoint; and significantly improve the technology readiness level (TRL) of critical spaceflight-enabling technologies. APL's program is directed at TRL = 4–6, which corresponds to a technology readiness horizon of ≈1–4 years. Thirty-seven projects in seven technology thrust areas were targeted. Nine of these projects are described in this article.

The Laboratory's ATD work has obvious benefits for the commercial space industry such as innovations in subsystems miniaturization. These benefits will lead to an overall reduction in satellite mass and power requirements and can result in decreased vehicle and propulsion costs. Exploiting its unique capabilities in space technology development, APL is a prime resource for assisting the commercial space industry in research and development efforts by maturing our ATD programs to the prototype and product development levels.

Linda A. Peregrino

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SECTION A. HIGHLY INTEGRATED ELECTRONICS

A1. Field-Programmable Analog Array Architecture

R. Timothy Edwards

APL's efforts in highly integrated electronics have focused on infrastructure requirements in spacecraft and instrument electronics. Our goal has been to reduce the resources (cost, mass, and power) necessary to implement circuit elements that are shared among multiple spacecraft and instruments.

Much of the cost of custom space-qualified electronics is not in the design stage but in the fabrication, packaging, testing, and qualification stages. The best way to lower the total cost of parts is to share them across multiple implementations by using parts that the user can configure (such as our field-programmable arrays) or that are flexible enough to meet the needs of multiple applications. This is the driving motivator for electronics development at APL under the ATD Program.

The arrival of digital field-programmable gate arrays (FPGAs) provided significant cost savings to the space electronics industry. These chips contain large arrays of simple, undedicated digital logic. End-users, by means of software, can connect the simple logic modules to make useful, powerful digital systems with design cycles of days. By contrast, custom design of integrated circuits (ICs) and board-level design using discrete components have design cycles of months. Custom circuits can be prohibitively expensive for many projects, and discrete component designs increase system size, mass, and power consumption. The same considerations apply to analog and mixed-signal (analog plus digital) circuit design. Almost all spacecraft contain numerous moderate-performance analog and digital processing and input/output circuits for applications such as status monitoring, motor control, temperature regulation, and signal conditioning and processing.

Field-programmable analog and mixed-signal arrays (FPAAs and FPMAs) address this need for quick turnaround time in analog flight hardware development. FPAAs vary widely in the choice of the core programmable modules. The granularity of the module tends to be a function of the performance of the interconnect. Slower (high-resistance, in the vicinity of 1 kΩ) interconnect types, e.g., those based on static random access memory (SRAM) or erasable programmable read-only memory (EPROM), can seriously degrade analog performance if inserted at arbitrary points in an analog design. Thus, modules for RAM-based analog arrays (e.g., an entire filter section) tend to have a large granularity and allow interconnect programmability only at certain critical points, for example, between filter sections or in series with the resistor in the amplifier's feedback loop. Faster (lower-resistance) interconnect types tend to have a finer module granularity, to the limit of gate array architectures, and allow programmability at the level of individual transistors but do not solve the problems of turnaround time and flight qualification. At an intermediate resistance, "antifuse" interconnect offers a good trade-off between functionality and performance on the one hand and quick development time and preflight qualification on the other.

APL entered into a cooperative agreement with Actel Corp.,[1] which is known for the manufacture of radiation-tolerant and radiation-hardened FPGA parts based on its patented antifuse technology. We designed an FPAA test chip that was fabricated in a 0.25-μm three-metal process, the same one used to manufacture one of Actel's commercial radiation-tolerant product lines.

Each programmable module incorporates circuit components as resources that can be connected into the circuit individually using antifuses. In the original unprogrammed state, the resources are decoupled from the circuit except through the small antifuse capacitance. When programmed, the antifuses form connections between module resources with resistances of 20 Ω or lower. The low resistance of interconnect paths allows us to reduce the granularity of our core analog module to individual components comprising

- 1 differential operational amplifier
- 4 programmable resistors (6 values in powers of 2, 1 to 32 kΩ)
- 8 programmable capacitor arrays (6-bit resolution, from approximately 0.5 to 31.5 pF)
- 32 analog switches (complementary pass gates)

Our test chip (Fig. A1-1) incorporates 12 modules in a 3×4 array. It can be used to implement many continuous-time and switched-capacitor circuits for standard spaceflight applications such as pulse shaping chains, analog-to-digital (A/D) and digital-to-analog (D/A) conversion, modulators, oscillators, and filters. Shift registers along the border of the test chip accept two bits that address an individual fuse by horizontal and vertical position, allowing external access to both sides of the selected antifuse for programming. There are over 30,000 programmable connections in the chip.

Actel's RT-SX process meets the stringent requirements of radiation tolerance for spaceflight applications. However, it is a process refined for digital circuits and not well suited to traditional analog circuit design. This necessitates careful consideration of the analog module design and layout. Fortunately, this aspect of analog design has

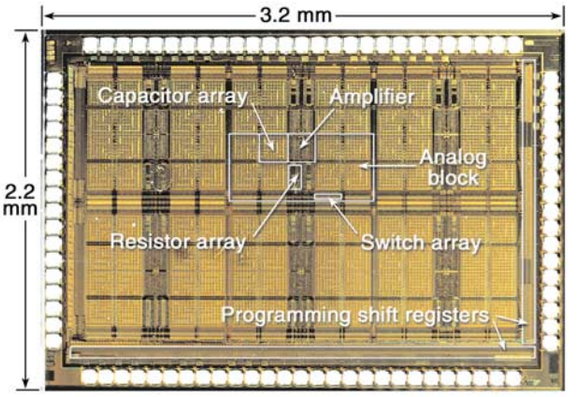

Figure A1-1. The fabricated test chip, showing 1 of the 12 analog modules and examples of its major components.

been a primary focus of research in recent years as a result of the wide availability of digital processes and the shrinking availability of dedicated analog processes. The research has produced, for instance, a wide variety of designs for CMOS operational amplifiers meeting our requirements for the FPAA. Our module amplifier is a two-stage differential design for a digital process (at 5 V), modified as necessary to maintain stability over the range of possible output loading capacitance that can be programmed into the module's capacitor arrays. The amplifier shows excellent performance for a moderately simple two-stage design without offset correction.

We have demonstrated the feasibility of programmable analog components for the aerospace industry, via a short development cycle, by using an existing state-of-the-art digital fabrication process. With technical goals met, taking the project from research to commercialization now rests with Actel and market forces.

Another possibility for programmable analog arrays is microelectromechanical systems (MEMS), otherwise known as "microfabrication" technology. Micron-scale nonvolatile mechanical switches can take the place of antifuses in similar FPAA designs and provide an even lower-resistance interconnect, with the potential for true in-system reprogrammability. This approach has a longer time to market, but we will be investigating designs and manufacturing techniques over the next 3 years in cooperation with a laboratory at the University of California, Los Angeles.

One important consideration of a second-generation system would be the inclusion of digital circuitry to form a true FPMA. The commercial potential for the FPMA lies in its ability to handle standard tasks usually implemented by digital signal processors (DSPs) or microcontrollers, a few of which have onboard A/D and D/A converters for interfacing to the exterior analog world. However, the FPMA can be optimized for each required task and thereby greatly reduce system complexity and power consumption. Low-bandwidth tasks such as temperature regulation can be combined on the same chip with high-bandwidth tasks such as signal conditioning, with each subsystem using only the resources it requires. Like the FPGA market (other than military and aerospace), its main use would probably be rapid design prototyping, after which the analog intellectual property core would be copied to a custom chip design for high-volume production.

Schedule, cost, and performance can also potentially be improved through the use of commercial fabrication facilities and processes rather than dedicated radiation-hard facilities. Specialized design methods and tools have been developed in our ATD effort to implement radiation-hard designs using commercial foundry facilities. We have developed several other promising technologies that can be used to dramatically lower the cost and risk of developing electronics for use in space. These technologies can also be used on Earth, and several are already being transferred to the commercial sector.

REFERENCE

[1]Actel Web site, available at http://www.actel.com/index2.html (accessed 22 Feb 2001).

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A2. Micro Digital Solar Attitude Detector

Kim Strohbehn, Mark N. Martin, and Stephen E. Jaskulek

Several advanced application-specific ICs (ASICs) have been developed under ATD to implement common spacecraft design and control elements. Of great interest has been the development of a microminiature digital solar attitude detector (DSAD) with a mass of 120 g. The detector can measure the Sun's position to better than 0.1° resolution using only 25 mW of power and transmits the digitized *x*–*y* coordinates over a simple serial interface. This groundbreaking part can also be used as a moderate-resolution monochrome imager, thus acting as a "postage stamp" imager.

Many proposed commercial missions depend on the use of "microsat" constellations to make simultaneous measurements at different orbital locations. Several new technologies are required to make the microsatellite concept viable from a mass and power standpoint. The apparent position of the Sun is an important spacecraft attitude measurement used by virtually all attitude determination and control subsystems. This measurement is commonly made with a DSAD. A micro DSAD (μDSAD) incorporating the entire sensor and its interface on a single chip would enable one to create a sensor small enough to be of great utility in microsatellites for spacecraft formation flying and would have applicability in nearly all NASA and commercial spacecraft missions.

Integrating the position-sensitive detector on the same chip as the support electronics is desirable but difficult and costly using a charge-coupled device (CCD) detector, so a detector compatible with CMOS processing is advantageous. Another disadvantage of most CCD detectors is the need for high-voltage, high-transient-current peripheral clocking circuitry.

APL has developed the first generation of such a μDSAD IC for use in microsatellites. The μDSAD design is based on our patented approach of combining a centroiding position-sensitive active pixel architecture with standard imaging capability for providing optional housekeeping images. The *x* and *y* coordinates of the light-intensity centroid are calculated on-chip, and can be directly read out of the chip over the simple serial interface. This approach avoids the need for a DSP in computing the position, thus dramatically lowering the required mass and power resources. Also, the design approach does not require any of the high-voltage, high-transient-current peripheral clocking circuitry needed by most CCD detectors.

The μDSAD realizes a significant breakthrough in meeting the requirements for the Sun sensor as part of ultra low power electronics and avionics. The μDSAD device can also be used as a medium-resolution imager for use in monitoring solar panel, boom, and antenna deployments or for sighting stars or other items of interest. Thus, one can view the μDSAD as a multifaceted breakthrough that meets several needs at once. Readout rates in either the Sun sensor or imager mode are limited primarily by image integration times and the serial output bus speeds. Approximately 5000 solar position readouts or image pixels can be read out of the sensor per second.

The μDSAD technology has been brought up to TRL 4. We have designed, fabricated, and tested a 64 × 64 pixel version of the μDSAD ASIC design (Fig. A2-1). Our layout style enables us to use commercial CMOS foundries and avoid the costly use of dedicated radiation-hardened processes. With this freedom, we have selected the AMI C5N 0.5-μm process for our designs, which is attractive since AMI is committed to maintaining it (longevity), and it is available for low-cost prototyping through the MOSIS service.

We have performed radiation testing on the prototype μDSAD chip. The apparent gain change after radiation was negligible, but we cannot measure absolute offset shifts with our current measurement equipment. It is clear, however, that the basic position-sensitive active-pixel method is quite radiation tolerant and has sufficient accuracy for a wide range of applications. A second chip, DSAD2, was dosed to higher than 300 krad and exhibited no apparent performance degradation. The test data on the DSAD2 test chip show that the

Figure A2-1. A test image taken with a 64 × 64 pixel version of the μDSAD ASIC.

annular *n*-channel transistor layout technique provides excellent total dose immunity with the 0.5-μm CMOS process. The DSAD2B prototype chip was tested for single-event latchup (SEL) at Brookhaven National Laboratory,[1] and was found to be SEL immune for a linear energy transfer of 120 MeVcm^2/mg. Using the prototype design, we have demonstrated robust performance, total dose radiation tolerance, and SEL immunity.

A full-featured 200 × 200 pixel μDSAD, designated DSAD3, has been fabricated with the same C5N process and is available for checkout. This chip requires only an external FPGA, a bypass capacitor, and appropriate optics to function as a DSAD sensor. It provides an I2C interface (four wires, including power and ground) and is predicted to dissipate less than 10 mW. The 200 × 200 μDSAD has several analog support circuits including a 10-bit successive-approximation A/D converter, an analog multiplexer, bias generation circuitry, a readout amplifier, a clock generator for the digital support circuitry, and a voltage reference. An SRAM chip will also be put on the test board to facilitate simple readout for the imager mode.

Using a simple single-element lens, the 64 × 64 pixel device was able to determine the Sun's position with 0.5° resolution over a 30° field of view (FOV); the larger 200 × 200 array should improve on both the resolution and FOV.

The DSAD IC has substantial commercial potential. We are in the process of entering into a license agreement with Barnes Engineering[2] (a subsidiary of B. F. Goodrich) to develop a commercial space product based on the ATD prototype. Barnes is collaborating with APL to perform the additional work required to bring it from TRL 4 to a flight-qualified design. By increasing the size of the array to 512 × 512 pixels, we believe we can achieve better than 0.1° resolution over a 100° FOV. The smaller arrays can view the same FOV with reduced resolution.

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[1]Brookhaven National Laboratory Web site, available at http://www.bnl.gov/ (accessed 22 Feb 2001).
[2]Barnes Engineering Web site, available at http://www.barnes.com (accessed 22 Feb 2001).

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SECTION B. SPACECRAFT MINIATURIZATION

B1. Integrated Power Source

Paul D. Schwartz, Aloysius F. Hepp, Binh Q. Le, Ark L. Lew, Sharon X. Ling, Michael F. Piszczor Jr., David D. Stott, Joseph J. Suter, and Bruce D. Williams

Miniaturization of electronics enables innovative low-cost space missions that require micro instruments and spacecraft. Missions that involve multiple, miniaturized spacecraft (see Chacos et al. and Lew et al., this issue) develop innovative sensing technologies that were impractical with conventional approaches. The miniaturization portion of the ATD Program has achieved a significant reduction in size, weight, and volume for implementing space-based electronics systems.

The cost-effective operation of a microsat constellation requires a fault-tolerant architecture that minimizes on-orbit operational costs by permitting autonomous spacecraft reconfiguration in response to unexpected fault conditions. APL has developed a power system architecture (Patent #6,157,167) that enhances spacecraft fault tolerance and improves power system survivability by continuously managing the battery charge and discharge processes on a cell-by-cell basis. This architecture is based on an integrated power source (IPS), which integrates dual-junction solar cells, a matrix of lithium ion battery cells, and processor-based charge control electronics into a multipurpose panel that can be used as a spacecraft side panel or deployed in place of traditional solar panels.

The 2.5-cm-thick IPS panel prototype (Fig. B1-1) provides thermal insulators and dedicated solar array and battery radiators to protect the lithium ion battery cells from the extreme temperatures of the solar cell layer. Simulation results confirm that the current IPS design will maintain the battery cells within proper temperature limits for all low-Earth orbits (Fig. B1-2).

IPS battery cells are arranged in matrices that are configured to meet application-specific voltage and

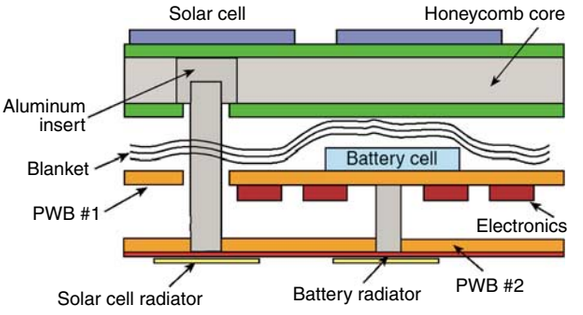

Figure B1-1. The 2.5-cm-thick IPS configuration provides thermal insulators, and dedicated solar array and battery radiators to protect the lithium ion battery cells from the extreme temperatures of space (PWB = printed wiring board).

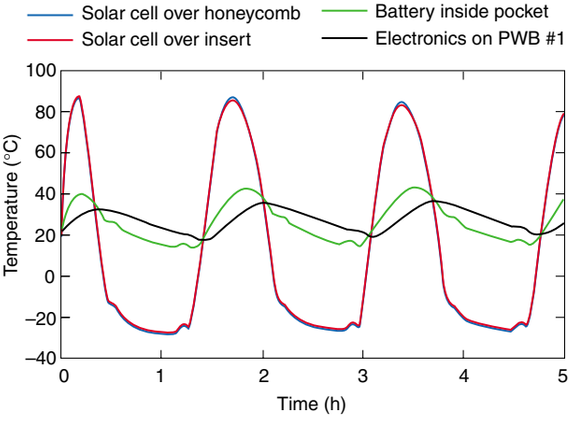

Figure B1-2. IPS solar array panel, 800-km nadir orbit, hot case.

load current requirements. The battery layer of the IPS prototype consists of a lithium ion cell matrix (26 VDC) and an array of lithium ion polymer battery cells. Although lithium ion and lithium ion polymer technologies offer high-energy densities, they require individual cell charge control that significantly complicates battery management. These requirements preclude the use of traditional architectures in which cells are arranged in a single stack and charged with a common electrical current determined by the state of the composite stack. In the IPS design, individual battery cell charge control based on simultaneous knowledge of the state of all battery cells is implemented to maintain cell-to-cell charge state equality in the absence of precisely matched cell characteristics.

In the IPS architecture, battery cells within a cell matrix are arranged in strings, with the charge and discharge current for each cell string set independently by the charge control processor. The processor sets the operating point of the solar array power source by controlling the sum of the battery string currents. Within each battery string, individual cells are shunted by solid-state control elements that are continuously programmed to bypass an appropriate portion of the string current to precisely maintain charge state equality.

The IPS charge control is based on the instantaneous charge current, cell voltage, and temperature of each battery cell. Using these data, the charge control processor continuously generates a coulometric record for each battery cell, which provides critical information for maintaining charge state equality. Additionally, coulometric data that are transferred to the spacecraft processor provide critical information for energy balance-based autonomous control software.

The charge current for a string with a failed battery cell can be set to zero by the charge control processor, leaving the full solar array current available for operational battery cells. Also, the charge control processor can be programmed to recognize and correct conditions that would eventually lead to cell degradation and failure. The processor software can be updated to permit the use of virtually any flight-qualified battery chemistry.

The IPS provides unregulated voltages that can be distributed to spacecraft systems and instruments in a traditional manner or used to power dedicated spacecraft loads through linear regulators or power converters. Critical and noncritical spacecraft loads can be powered from independent power sources, further improving spacecraft fault tolerance and reducing microsat constellation operational costs. In addition, eliminating the shared power lines between spacecraft systems and instruments eliminates the conducted power line noise coupling that is typical of traditional architectures.

The development of a prototype unit of a multipurpose IPS panel shortens the miniaturized spacecraft development cycle and enables low-cost constellation missions. Furthermore, the electronics concepts used in developing the IPS can be easily transferred to other applications (e.g., electric vehicle charge control).

IPS prototype development has progressed through the design and fabrication stages, with software development and flight unit qualification remaining. Patent protection has been granted for the IPS concept and for the IPS electronics architecture.

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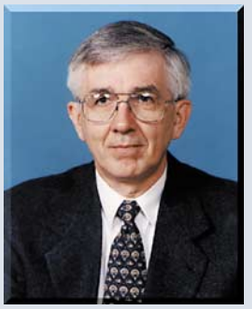

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Section C. Spacecraft Communications

A significant challenge in the advancement of spacecraft is the improvement of the radio-frequency (RF) communications capability onboard the spacecraft. Technology development in communications is made difficult by two critical constraints: (1) the achievement of higher bit rate performance is limited by fundamental laws of physics and communication theory, and (2) the miniaturization of communications hardware is limited by the expense associated with operating at very high frequencies, typically in the microwave region. The objective of this ATD Program area was to develop the architectures and technologies necessary to minimize the effects of these constraints, allowing infusion into commercial and scientific flight programs.

C1. K_a-Band Hybrid Inflatable Dish Antenna

Cliff E. Willey, Robert S. Bokulic, William E. Skullney, and Ron C. Schulze

Inflatable antennas are the subject of current space research because of their potential for enabling high bit rate communications.[1] However, a significant problem associated with inflatable technology is the "all-or-nothing" scenario, where the success of the mission depends on successful deployment of the antenna. Therefore, the application of inflatable antennas is currently limited to missions where a very large aperture is needed (e.g., interstellar probes, large imaging radar satellites). APL is developing a new inflatable antenna concept that can be integrated into spacecraft missions on a shorter timescale than would be possible with other inflatable antenna approaches.

This concept has been developed as a hybrid approach that avoids the all-or-nothing scenario by providing a backup capability in the event of inflation failure. The antenna system combines a fixed parabolic dish with an inflatable annulus to greatly increase the reflector size on orbit (Fig. C1-1). The fixed parabolic dish provides a "risk buffer" whereby a high-gain capability is retained, even in the event of inflation failure. A dual feed ensures operation of the smaller fixed dish throughout the mission. The inflatable annulus is stowed compactly under the fixed dish to fit a variety of spacecraft and launch vehicle envelopes. Moderate gas pressure deploys the annulus, which forms a parabolic reflector surface.

Shortly after inflation, the composite materials that form the annulus surface are made rigid by thermoset, ultraviolet, or other curing methods. This concept might be applied to a typical 1-m dish to increase its diameter to 4 m or more. An inflated 4-m flight antenna could return a bit rate on the order of 1 Mbps from Mars with a 30-W K_a-band amplifier. A major challenge is achieving a reflector accuracy on the order of $\pm$0.5 mm to ensure proper operation at K_a band (32 GHz).

Our ATD activity is a collaboration between APL and ILC Dover, Inc.[2] We have focused on the construction of a breadboard hybrid inflatable antenna. The breadboard, currently being built by ILC Dover, will be a 2-m-dia. parabolic dish designed to demonstrate that the surface accuracy required for K_a-band operation can be achieved. It consists of a 0.5-m-dia. rigid reflector surrounded by a 2-m-dia. inflatable annulus. Upon inflation, the shape of the annulus will be precisely determined by optical measurement techniques. The surface measurements will be used to calculate the errors between the inflated surface and the tooling used to create it. We will also be able to project the efficiency of the inflated annulus.

Development of this hybrid antenna concept provides APL with a scalable high-gain antenna architecture that can be applied to future government and commercial spacecraft missions. It yields enhanced RF performance over fixed dish antennas by greatly

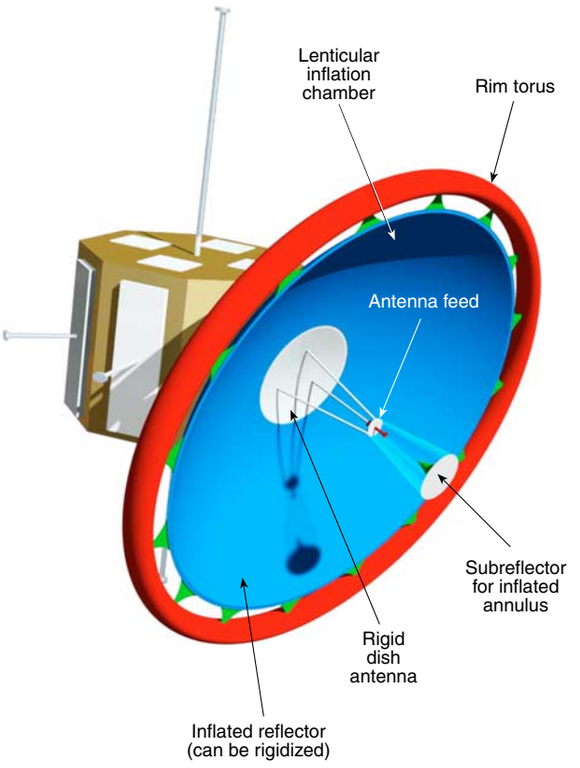

Figure C1-1. Hybrid inflatable antenna in its deployed configuration. This concept avoids the "all-or-nothing" problem commonly associated with inflatables.

expanding the reflector surface. For example, a 4-fold increase in the diameter of this antenna results in an up to 16-fold increase in the volume of data for space missions. The inflatable antenna stows very compactly, allowing missions to use smaller and less expensive launch vehicles. It is potentially lighter than a large fixed or deployable antenna, thus reducing spacecraft subsystem mass and providing more mass for spacecraft payloads. A significant cost saving is possible for this design versus mesh-type deployable reflectors because the deployment system is simple and can use existing spacecraft subsystems for gas deployment.

Multiple benefits can be achieved from developing precision inflatable space structures. The new technology has great potential for increasing RF gain and decreasing mass and cost relative to existing technologies. These benefits can enable spacecraft missions that have increasing demands for power and data. Inflatable solar arrays, solar sails, and optical systems can benefit from the advances being made on our project. The hybrid inflatable antenna is an important evolutionary step toward getting flight demonstrations of this emerging technology.

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C2. K_a-Band MMIC Phased Array Components

John E. Penn

Satellite communications have evolved to higher and higher frequencies as communication rates and requirements have increased. NASA's Deep Space Network (DSN) is used to communicate with spacecraft across the solar system. NASA is working to advance the DSN's communications capability from X band (about 8 GHz) to K_a band (about 32 GHz), mainly to achieve higher data transmission rates for the same transmitted power level. With all other parameters held constant, a K_a-band system would provide 16 times as much data as an X-band system. In practical application, a data rate improvement factor of 4 can be achieved. Bandwidth as a percentage of carrier frequency would increase 4-fold by the switch from X band to K_a band. For a spacecraft in deep space with limited power resources for communications, it is easy to see why there is interest in increasing the science return by going to K_a band. However, designing efficient power amplifiers at K_a band is considerably more difficult than designing at X band because of the close tolerances involved and the lower efficiencies of the devices.

Given that microstrip and connector losses tend to be higher at K_a band, one way to improve amplifier efficiency in a phased array is to use spatial combining, which is extremely efficient compared to lossy combiner networks. Many small, highly efficient K_a-band amplifiers can be combined in a large phased array, resulting in a system that degrades gracefully with amplifier failures and provides a combined RF power equal to the sum of the individual elements. Two key components in a phased array are the power amplifiers and the phase shifters, which allow the focused beam pattern to be steered.

Under the ATD Program, we have designed and built custom microwave monolithic ICs (MMICs; Fig. C2-1) for a very efficient K_a-band power amplifier and a K_a-band 4-bit digital phase shifter. These two components are critical in a phased array design. MMICs for K_a-band (32-GHz) power amplifiers are difficult to find, and those that are available are not very efficient. We have designed such a power amplifier and completed first-pass fabrication at the TriQuint/Texas[1] foundry. The first-pass results are good (Table C2-1); a power-added efficiency (PAE) of nearly 30% was achieved.

At present, no known commercial MMIC phase shifters are available at the desired K_a-band frequency of 32 GHz. Each phased array element must have a

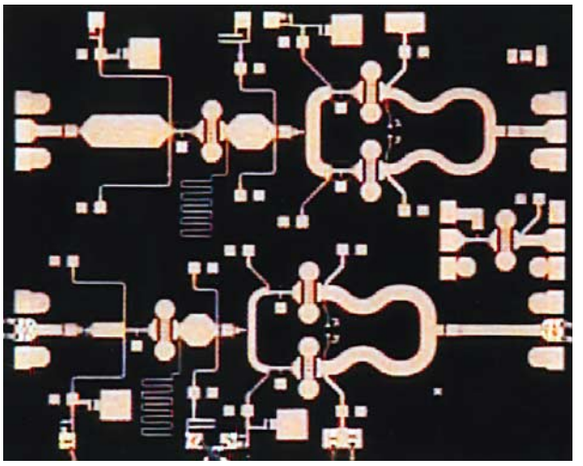

Figure C2-1. The K_a-band solid-state power amplifier, which was designed under the ATD Program, produced a 29% PAE.

Table C2-1. K_a-band MMIC power amplifier goals vs. performance (first foundry pass).

Parameter	Goals (optimized at 32 GHz)	Measured (30 GHz)
Gain (dB)	12–14	14–15
Power out (dBm)	27	>27
PAE (%)	30	28–29
Voltage	6–8	6–8

controlled phase shift relative to the other elements to focus the beam toward the receiving antenna. Important parameters for a phase shifter include the number of bits or steps of phase shift, insertion loss balance between phase states, accuracy of phase shifts, total insertion loss of the phase shifter, and bandwidth.

During the design of the 4-bit phase shifter, different topologies were explored for each of the 180°, 90°, 45°, and 22.5° bits. The nominal 22.5° bit used the Lang coupler with a tuned switched reflection for a wideband 22.5° phase shift. A much smaller alternate 22.5° field-effect transistor (FET) bit used a differential phase shift from two FETs with opposite gate control voltages to provide broadband phase shift. This alternate compact 22.5° topology provided excellent results.

Trade-offs of the various topologies appropriate to each phase shift bit were performed to minimize insertion loss imbalance, reduce total insertion loss, and provide accurate wideband phase shift. Accurately predicting phase at K_a band is generally much more difficult than estimating insertion loss. Agilent's EEsof simulator was used for much of the initial design process, and electromagnetic simulators like Sonnet and Ansoft's high-frequency structure simulator were used to provide a more accurate analysis of the best design candidates.

We have also completed first-pass fabrication of the 4-bit K_a-band phase shifter at the TriQuint/Texas foundry. The results (Table C2-2) are very promising. More design work and a second foundry pass will be required to optimize the design.

Few commercial K_a-band MMIC power amplifiers exist, and even fewer are power efficient. Typical commercial K_a-band MMIC amplifiers are 15–23% PAE. Space applications will require efficiencies of 30% or more. The 30% PAE achieved by these 0.5-W efficient power amplifiers is as good as the best commercially available K_a-band MMIC amplifiers. Customizing MMIC amplifiers to a specific program or need will often produce superior results compared with an off-the-shelf component.

Again there are no currently available MMIC phase shifters for the K_a band. A broadband, compact 4-bit MMIC phase shifter could have many commercial applications, from array systems in ground-based local multipoint distribution service systems to spacecraft K_a-band communications. For comparison, a single 180° 4-bit K_a-band phase shifter developed for 26-GHz operation by Harris for a NASA program has nearly as much loss and occupies almost as much IC area as this 4-bit 28–36-GHz phase shifter. A second-pass K_a-band phase shifter is currently being fabricated which should improve the phase accuracy and insertion loss balance over the initial first-pass design.

Table C2-2. K_a-band MMIC phase shifter preliminary results at 32 GHz (first foundry pass).

Bit (deg)	Phase shift	Insertion balance	Insertion loss (dB)	Notes
180	170	0.1	≈3	Measured as a single bit
90	104	≈3[a]	N/A[b]	Measured in overall 4-bit configuration
45	68	≈0.7	N/A[b]	Measured in overall 4-bit configuration
22.5	35	0.5	1.0–1.5	Measured as a single bit
22.5 HLP[c]	23	≈0.2	1.0–1.5	Measured as a single bit

[a] The cause of the high insertion loss balance is due to modeling errors. There was a large difference between the electromagnetic simulation and the original linear simulation.
[b] Not available as individual test bits.
[c] High-pass/low-pass implementation.

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SECTION D. ADVANCED SPACECRAFT ARCHITECTURES

D1. 1394 Serial Bus

Martin E. Fraeman

APL is improving the use of the IEEE 1394 serial bus for subsystem communications on spacecraft. IEEE 1394 is well suited for this purpose because its protocols are robust and rigorously defined, throughput is large but power consumption is modest, and redundant configurations are feasible when needed to support missions of long duration. We are also assessing the survivability of several interconnect topologies. Spacecraft system designers can use these results to balance redundancy and cost against mission requirements. We are particularly concentrating on algorithms to permit multiple IEEE 1394 buses within a spacecraft to communicate. Using several buses on the spacecraft increases available bandwidth and isolation among subsystems, and eases development. Our goal is to investigate the feasibility of developing a bus interface that integrates these functions onto a single chip.

APL is using the IEEE 1394 high-performance serial bus standard to implement fault-tolerant satellite electronics. IEEE 1394 defines techniques for serial digital data communications among multiple nodes. Two interconnect environments, cable and backplane, are specified. The cable profile is generally used to connect nodes in separate chassis; the backplane profile is used to transfer information among nodes that share a common housing. APL participated in the development of IEEE 1394 and has been using it since the standard was first approved in 1995. The Space Department has used the capabilities defined by the standard's backplane profile to design fault-tolerant electronic subsystems. Although our applications were intended for use on satellites, the technology we are developing can be applied to any function that requires fault-tolerant and power-efficient data transfer between circuits within a common chassis. Our current design will operate at data rates up to several hundred million bits per second and is primarily limited by signal integrity effects rather than semiconductor technology.

Development of a dual-channel IEEE 1394 backplane profile bus interface unit (BIU) IC was initiated by an APL IR&D project in 1996. The project was part of a larger effort to develop a fault-tolerant spacecraft integrated electronics module (IEM; see Lew et al., this issue). Preliminary versions of the IEM have already been used on the APL-developed Thermosphere-Ionosphere-Mesosphere Energetics and Dynamics (TIMED)[1] and CONTOUR[2] spacecraft. The IEM merges several traditional satellite functions within a single chassis. Resource reuse and sharing are encouraged by the IEM concept. IEEE 1394 and the BIU chip will be used to transfer data among circuit boards in a future internally fault-tolerant version of the IEM. This IEM uses redundant circuit boards to avoid system failure despite the occurrence of faults. In case of board failure, a backup copy of the board replaces the failed unit. This scheme also requires redundant data communication channels since faults may also occur within those networks. Hence, the BIU chip interfaces with two independent IEEE 1394 serial buses, one as a primary data bus and the other as a secondary bus

to replace a failed primary bus. The chip includes two independent channels, with packets transferred through on-chip memory buffers. Data from both channels are transferred to the rest of the node through a configurable-width (8, 16, or 32 bits) parallel memory data bus.

Unlike other implementations of IEEE 1394, the APL BIU chip design can perform data transfers without requiring a host microcontroller. A BIU chip configured to operate in this "remote mode" does not use a processor to interpret data packets addressed to that node. Instead, logic in the chip decodes each packet it receives and performs the indicated read or write transaction to the node's address space. After the transfer is completed, the BIU chip hardware assembles and issues a response packet over the serial bus to the requestor node. The BIU chip can also be used in a more traditional "host mode" where a local microcontroller formats packets for transmission and decodes and interprets received packets.

A very high speed IC hardware description language–based BIU design has been written, synthesized, and simulated. A test bed that incorporates four bus nodes has been built. The test bed implements a prototype of each node in a FPGA. Host processors control two test bed nodes that operate in "host mode." The other nodes operate in remote mode and transfer data directly between node local address space and the bus without any external computer support. However, the host processor does have independent access to the local node address space so that the proper operation of BIU chips in remote mode can be verified. The prototype implementation of the dual-channel BIU design fits in less than 300,000 gates and 80 kbits of memory, well within current radiation-hard ASIC fabrication capabilities. The test bed has been used to extensively exercise the BIU design. All operating modes and features have been exercised and are fully functional.

After completing this initial design, we identified several desirable enhancements for spacecraft as well as other fault-tolerant applications. Our ATD Program has implemented the logic of most of these improvements. Additional capabilities include a method to extend the backplane profile across a small number of electrically isolated segments, automatic transfer of large blocks of data using multiple packets among remote-mode nodes, a programmable link/physical layer clock ratio to enable much higher-speed bit rates, and better support of bus monitoring/stimulation to improve onboard fault detection and ease system integration testing.

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SECTION E. INSTRUMENT-ENABLING TECHNOLOGIES

E1. Miniature Mechanisms Tool Kit for Micro Spacecraft

Cliff E. Willey, Brett Huettl, David Dowen, and Stuart W. Hill

Spacecraft all share the common purpose of delivering carefully constructed measurement technology: the instruments. Ultimately, the success of a mission depends on the ability of instruments to make the measurements that drove the mission's creation. Because of the stringent requirements on spacecraft instrument reliability, fault tolerance, mass, and power consumption, instrument design and fabrication have developed into specialized

fields of expertise. Instrument development has required extensive rethinking of original techniques. Today ambitious goals for space missions necessitate even more extensive development of the technologies that both enable instruments to function and enable the synergy of instruments with their supporting spacecraft.

With the current push for microsatellites in the range of 10 to 100 kg comes a new era in mechanism design. Advances in the variety and processing of materials have created abundant opportunities to miniaturize mechanisms. Although many off-the-shelf mechanisms are very compact, they do not yield the order-of-magnitude reduction in size needed for microsatellites. This ATD project focuses on the design and development of six miniature mechanisms that form a satellite "tool kit." Jointly developed by APL and Starsys Research Corp.,[1] the mechanisms (Fig. E1-1) include a micro and mini separation nut, a mini rotary actuator, a mini burn wire release, a shaped memory alloy (SMA) linear actuator, and an SMA redundant release mechanism. All of these mechanisms are scalable and show promise for additional miniaturization.

The mini separation nut (Fig. E1-1a) was designed to restrain and release a small screw. The separation nut is similar in design to conventional devices with a segmented nut constrained by a collar. With the collar in place, the segmented nut is maintained in the shape of a nut, allowing a mating screw to be threaded and tightened in place. The collar is maintained in position by a compression spring that prevents it from moving because of vibration loads. The collar is driven in opposition to the spring by an SMA element, which is heated directly or can be designed with a resistance heater directly attached to the SMA element. To release the screw, power is supplied to the heater or SMA element. As it is heated through its transformation temperature, the element recovers previously induced strain and drives the collar to allow the segmented nut to separate, releasing the screw. When power is discontinued, the mechanism can be manually reset.

The micro separation nut (Fig. E1-1b) uses a single SMA band that has been formed into a circular shape. The mechanism is set by inserting the screw through the housing and past the inner diameter of the SMA spring. The cap holds the SMA spring properly in the housing. The SMA spring is manually compressed from two sides until it is secure around the screw. The mechanism may then be preloaded and is ready for release. When the SMA spring is heated, it returns to its circular shape, releasing the screw.

The mini rotary actuator (Fig. E1-1c) provides 0.042 N-m of torque in two directions over a 120° rotational range. The rotary actuator can be used to open and close a small instrument or camera cover and includes a detent latch that can maintain the cover in either the open or closed position without the use of power. The holding torque for either of the two positions is equal to or slightly greater than the output torque of the rotary actuator. The design uses an SMA torsion spring wound past its nominal position to rotate the output shaft. As heat is applied, the spring returns to its nominal position, providing the output torque. This motion drives the output shaft through 120°, at which point the detent engages. Power is then discontinued, and the rotary actuator remains in the open position until the opposite side is operated.

The mini burn wire release mechanism (Fig. E1-1d) was developed at APL for a miniature instrument cover or similar device needing an extremely compact, low-mass, and low-power actuation device. It uses a burn wire to directly carry the tensile load of a cover or screw that is attached to its retainer. Current applied to the wire breaks or fuses the wire at the location of the retainer, releasing the hardware attached to it. This differs from other types of satellite burn wire releases in that this mechanism uses the wire to directly carry the tensile load, making it a highly simplified design that can be greatly miniaturized. The design can also be easily scaled up or down according to the requirements of the device to which it is attached. The burn wire release mechanism has only five components, one of which is released with the cover. These components are also multifunctional. The burn wire is used to hold the mechanism together, carry the restraint load, make electrical connection, and initiate the release action. The size of the wire is based on restraining a 100-*g* cover. The rest of the mechanism is designed to be packaged as compactly as possible and to provide thread for a small screw. A kick-off compression spring is incorporated to overcome friction.

Linear actuators are prevalent in satellite programs as triggers or switches for mechanical devices. The mini linear actuator being developed at APL is designed to provide a quick-acting, low-shock linear motion. A single test unit has been built (Fig. E1-1e). This prototype mechanism uses SMA wire to actuate a high-force, low-shock pin puller that can trigger a number of latch devices on instrument shutters or covers. It is self-resettable using a bias return spring and can operate in flight for numerous actuations.

The motion (or strain) of typical SMA materials is limited to 8% of the material length. A nominal design for this mechanism would limit strain to 2% to ensure adequate fatigue margin. Larger stroke length can be achieved if room is available across a cover or down the side of a telescope for a longer SMA wire. Redundancy can be designed into the system with dual wires that can be individually powered and can singularly operate the device.

The SMA nickel-titanium wire is directly heated by running current through it. Although the device is not

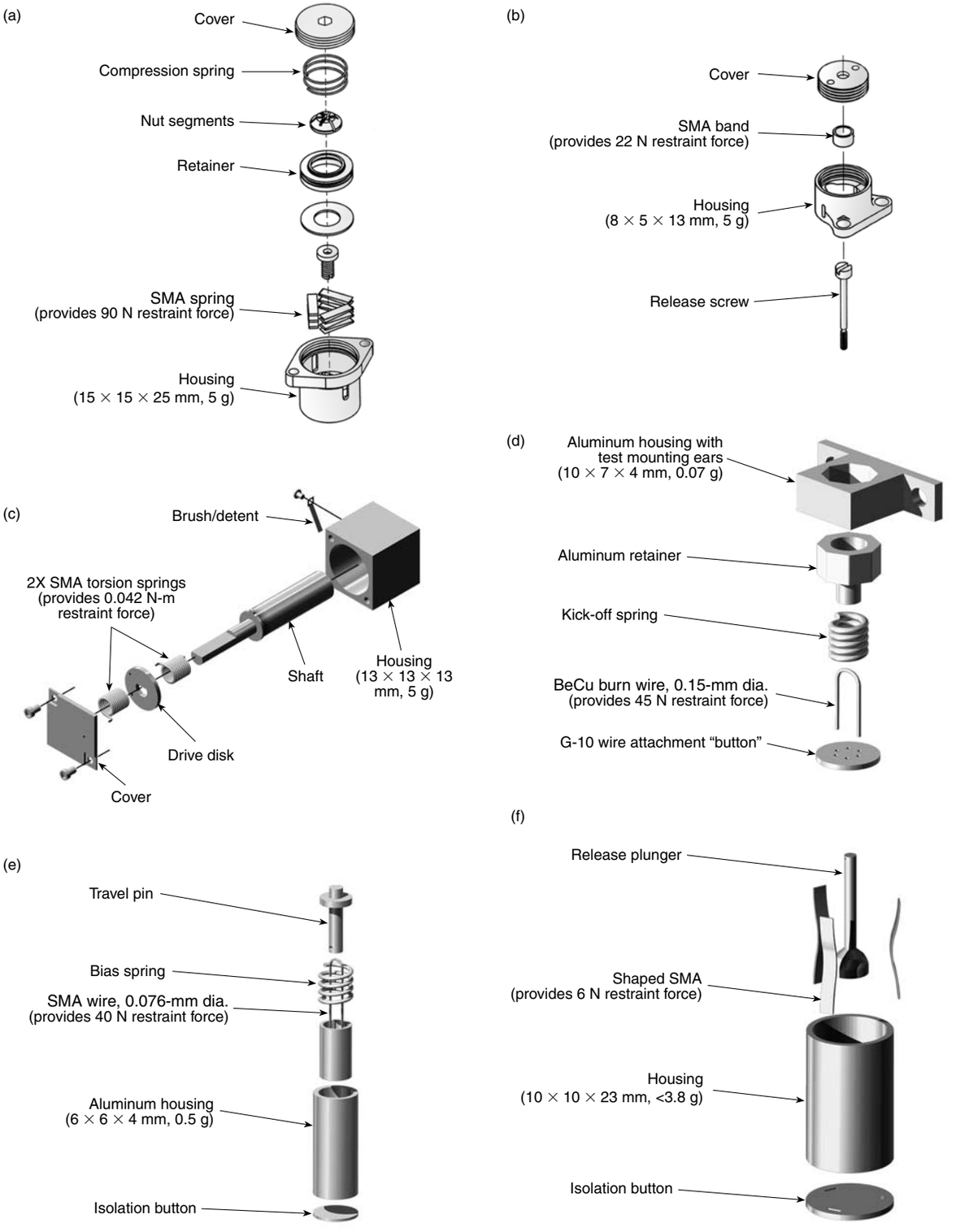

Figure E1-1. Miniature mechanisms developed by the ATD Program. (a) mini separation nut, power = 2–5 W; (b) micro separation nut, power = 2 W; (c) mini rotary actuator, power = 2–5 W; (d) mini burn wire release mechanism, power = 5–8 A at 6.5 V; (e) SMA linear actuator, power = 0.25 A at 8.5 V; and (f) mini redundant release mechanism, power = 2–5 W.

too sensitive to its external thermal environment, when heated, its response time can be less than 1 s. Through a strain recovery process in the material, the wire contracts when heated and returns to its original shape when cooled using a compression bias spring. It is a self-latching device that is fully and repeatedly testable.

The mini redundant release mechanism is designed to provide both electrical and mechanical redundancy. Most mechanisms strive for redundancy in the electrical connections but have single points of failure in mechanical operation. This mechanism provides multiple redundancies with its ability to function (release a plunger) with two of the three SMA elements operating. The mini redundant release is in an early stage of development, with one test unit built (Fig. E1-1f). This prototype mechanism contains shaped SMA strips that lock a restraint shaft for an instrument cover, solar array, or other system needing a release device. SMA strips grip the end of the shaft while in a cold state. When powered and brought to a higher temperature, the SMA strips change shape to "open the lock."

Full mechanical redundancy is achieved because the device still operates if one of the strips fails to open. A resistor heater on the housing provides the temperature control. This design can be converted to direct current heating to increase response time. Direct current heating will also provide further electrical redundancy. This mechanism can be miniaturized further, depending on the holding force required.

The key factor in this project for shrinking mechanism size is to reduce complexity. The mini separation nut design was taken from a conventional separation system and was simply scaled down. It was judged to be not quite miniaturized for the micro satellite uses that were envisioned. By radically redesigning the mini separation nut, the micro separation nut was able to get the performance needed with three components instead of eight and was 75% lighter and smaller than the mini separation nut. Another example is the burn wire mechanism, which is the smallest and lightest in the tool kit owing to its simplified and streamlined design. It is this kind of streamlining that is needed to address micro satellite needs.

Some of these mechanisms give up redundancy for simplicity. This may be a risk that constellations of small and inexpensive micro satellite constellations will be willing to take. If redundancy is required, there are options in this tool kit that provide it. Micro mechanisms must break from traditional mechanism design to meet the need of future micro satellites.

The problems encountered in this project were not completely addressed or fully tested. Continuation of the effort is expected to look in more detail at manufacturability, assembly, characterization of SMAs, and power and mass optimization for these mechanisms. From the brief testing performed, there appear to be attainable solutions to all the problems encountered. Future work should yield mechanisms that are qualified for flight. These will be some of the smallest and lightest mechanical components available that provide precise and consistent performance for micro satellite as well as traditional satellite programs.

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SECTION F. MISSION AUTONOMY

F1. Autonomous Solar Navigation System

Yanping Guo

A completely self-contained autonomous solar navigation system has been developed for interplanetary space missions. The system uses only onboard observations of the Sun in combination with onboard spacecraft attitude data to estimate and predict the spacecraft's orbit autonomously. Unlike the current ground-based navigation system, which uses two-way coherent radio Doppler tracking through the Deep Space Network (DSN), this system does not need the DSN or any control from the ground, allowing it to navigate independently. In addition, since the Sun is an active energy source and visible everywhere in the solar system and beyond, the system is applicable to spacecraft moving nearly anywhere in space.

Navigation plays a critical role in deep space missions since a spacecraft launched to a planet, asteroid, or comet must be accurately navigated to reach its destination in a close flyby with, orbit at, or landing on the targeted body. Autonomous spacecraft navigation is highly desirable, especially for missions that require updates of a spacecraft's position in real time and frequent thrust and trajectory adjustments (e.g., missions that use solar electric propulsion or solar sails). It can increase the spacecraft's capability and flexibility, taking immediate action in critical situations without any two-way light-time delay, thereby increasing the spacecraft's survivability and reducing risk. It also reduces mission operation costs, with daily manual operation being replaced by onboard autonomous operation.

The Autonomous Solar Navigation System has unique and appealing features for broad application. Its use of the Sun as the navigation reference allows it to be employed in any mission exploring the solar system, and even for missions to nearby stars. It can be used for interplanetary space missions as well as missions to explore the Sun. Even for Earth satellites that can communicate conveniently with Earth-based navigation systems (e.g., DSN, Global Positioning System), this jam-proof system offers an alternative solution. Its complete self-containment makes it invulnerable to any destructive interruptions from the ground, such as high impulsive electromagnetic fields or jamming radio signals. Aside from its main function as a navigation system, it has other applications. For example, it can potentially find the Earth's location after a spacecraft "wakes up" from a safe mode and provide the spacecraft with high-accuracy Earth direction for optical communication.

The spacecraft's state (position and velocity vector) is determined by processing the solar observation data onboard. Two types of solar data can be used for estimating the state of the spacecraft:

1. The directional data that measure the change in the Sun's direction as a function of time, viewing the Sun from the spacecraft against the star background
2. The optical Doppler shifts observed in sunlight that provide the line-of-sight velocity of the spacecraft relative to the Sun

All of the six orbit elements that define a spacecraft's orbit can be completely determined with measurements of the Sun's direction vector as a function of time. The use of optical Doppler data in addition to the directional data, though optional for orbit determination, adds a constraint in the dimension perpendicular to that given by the directional data. Inclusion of the optical Doppler data in the orbit determination process can speed up the convergence of the orbit-fitting process and improve the orbit solution.

APL designed a dual-mode imaging system (Fig. F1-1) for measuring the direction of the Sun using a CCD camera which captures the image of the Sun against a background of stars. The stars appearing in the Sun's image frame serve as a direction reference. A conventional optical imaging system, which is designed for imaging planetary bodies, cannot be directly used for taking the Sun's image because the Sun is much brighter than the planetary bodies. Our design modifies the conventional system by controlling the intensity contrast of light coming from objects with large differences in brightness. The designed image system can take pictures from both planetary bodies and the Sun by operating in two modes: as a regular imager when imaging planetary bodies or as a Sun imager when imaging the Sun.

The practicality and feasibility of using solar navigation was assessed by applying it to a real space mission. The Solar TErrestrial RElations Observatory (STEREO) mission[1,2] was selected as a case study because its available onboard science instrument (the Solar Coronal Imaging Package) can measure the Sun's direction with no additional hardware. The STEREO mission, which will be launched at the end of 2004, will provide a new perspective on solar eruptions (coronal mass ejections) and their consequences for Earth by imaging the ejections and background events from two spacecraft simultaneously.

We performed computer simulations on orbit determination based on the STEREO mission trajectory profile and onboard instrument and system capabilities.

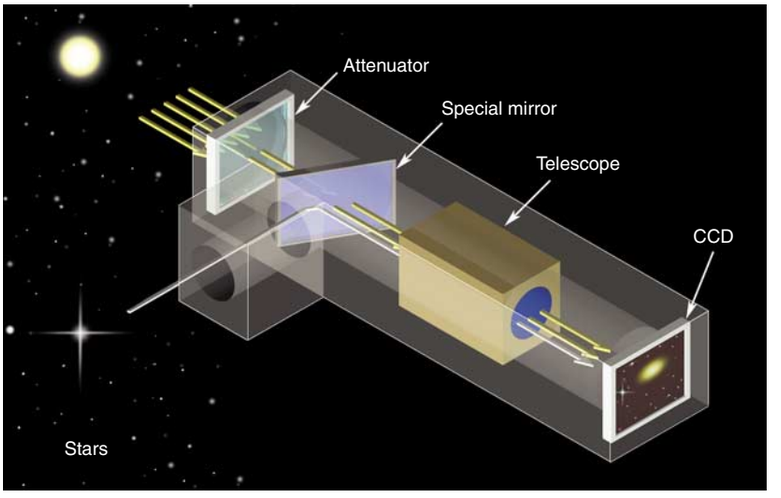

Figure F1-1. A dual-mode imaging system designed to take pictures of the Sun or planetary bodies against a background.

Sun direction measurement errors contributed from the science instrument and guidance system were considered and folded into the simulated observation data. The simulated Sun direction data were used to estimate the spacecraft's position and velocity vector. Promising results on orbit determination were obtained from the simulations, showing that the mission-required orbit solutions can be achieved using autonomous solar navigation. An in-flight test of a prototype of the solar navigation software package on the STEREO mission has been proposed.

Solar navigation has demonstrated real space mission feasibility and comparable navigation accuracy with the instrument technology used in the studied cases. Given its unique ability, self-containment, and universal applicability—benefiting from technology development and innovation in instruments and sensors—autonomous solar navigation is very promising and has great potential for enhancing spacecraft performance for space exploration.

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SECTION G. MODEL-DRIVEN IMPLEMENTATION

G1. Spacecraft Modeling and Simulation Standards

Andrew D. Goldfinger

Spacecraft design has matured to a point where commercial design tools are regularly used and their development has become a lucrative industry. Products such as Analytical Graphics' Satellite Tool Kit and various specialized design packages for Mathworks' MATLAB are in routine use. Yet the overall spacecraft design process remains cumbersome and inefficient. Modeling and simulation, which hold great promise for increasing efficiency and cost-effectiveness, are often done in a piecemeal fashion, a mixture of legacy and custom standalone codes for various subsystems communicating with one another haphazardly ("sneakernet").

To correct this situation, we have a vision. A designer has an idea for a spacecraft. Armed with the requirements, he seeks subsystem configurations that will accomplish the mission. He searches a knowledge base for previous designs, finds an attitude system that comes close to meeting his needs, and obtains and executes a simulation of it. But the reaction wheel (a type of attitude actuator) exerts a torque that is too small, so an alternative must be found. Browsing the Web, he finds that the ACME Corp. markets a wheel that might be adequate. He downloads a simulation of this component and, since it has been written to conform to industry-wide standards for reaction wheels, it fits effortlessly into his attitude subsystem simulation. Finding that the ACME wheel meets his torque needs, he tries to determine what impact it will have on the spacecraft's power consumption and thermal management. He interfaces his attitude subsystem simulation with software models of the power and attitude subsystems and, since they too have been written to industry standards, all three interact easily. More subsystems are added, and soon the designer has developed a *virtual spacecraft* that emulates the behavior of the actual spacecraft being designed. As development continues, actual pieces of spacecraft hardware are tested by plugging them into the virtual spacecraft, where they replace the corresponding software simulations.

For this scenario to work, the industry-wide standards for spacecraft simulation must first be developed. To this

end, APL has been conducting an ATD project to begin the definition of these standards. We started by studying three dissimilar spacecraft with the goal of discovering their commonalities. These spacecraft are TIMED,[1] a near-Earth environmental sensing system in the design phase, Midcourse Space Experiment (MSX),[2] a large multisensor mission currently in orbit, and the Near Earth Asteroid Rendezvous (NEAR),[3] a deep space mission to the asteroid Eros that ended recently.

In examining these spacecraft, we found that it was desirable to decompose each along both functional and physical lines. Functionally, each spacecraft could be divided into the classical nine subsystems: attitude determination and control, C&DH, instruments/payload, mechanical and structural, navigation, power, propulsion, telecommunications, and thermal management. In turn, each of these subsystems could be functionally decomposed into components, creating a set of hierarchical relationships we refer to as "has-a." Thus a spacecraft "has-a" attitude system, which in turn "has-a" reaction wheel (Fig. G1-1).

Decomposing the spacecraft physically, we found that there were categories to which the components belonged. For example, a reaction wheel has the physical property of mass along with the physical property of drawing power from the power subsystem. We call the relationship between the functional component and its physical properties "is-a." Thus a reaction wheel "is-a" massive object, and it "is-a" powered object.

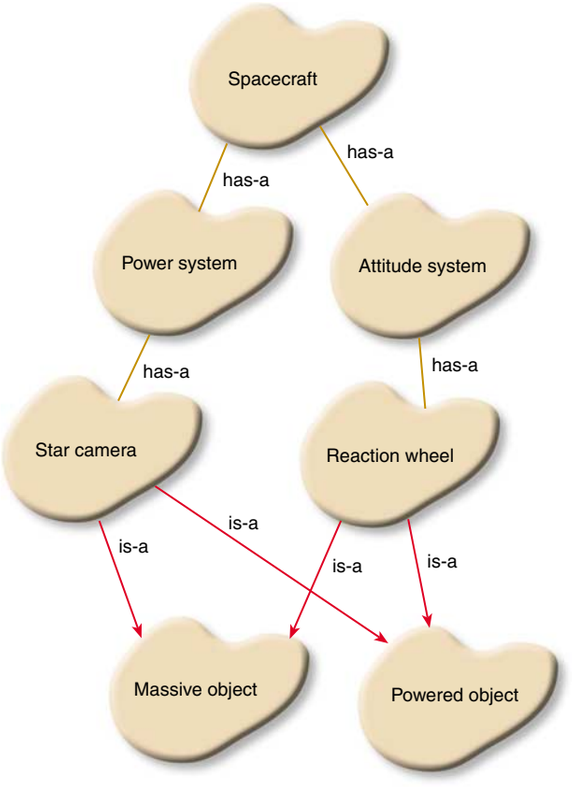

Figure G1-1. A simplified attitude control system showing component interactions. The reaction wheel adheres to the massive object standards, and the star tracker adheres to the data object standards.

We have chosen to construct our standards using an object-oriented perspective. Thus, a reaction wheel object is an instantiation of the abstract *reaction_wheel* class. This class inherits attributes and methods (loosely speaking, commands) from those classes to which it bears an "is-a" relationship. Hence, the *reaction_wheel* class inherits attributes and methods from the *massive_object* and *powered_object* classes. Typical attributes are *mass* and *position* from the *massive_object* class and *power_drawn* from the *powered_object* class. In addition to attributes that are inherited, the *reaction_wheel* class has attributes of its own such as *reaction_wheel_speed*.

Besides defining standards for component classes, we needed to provide objects that simulated the environment and physical reality that interacted with the subsystems and components. For example, as part of the standards a *spacecraft_dynamics* object must be provided, along with *magnetic_field* and perhaps *atmospheric_drag* models. These standard "glue" objects interact with the functional components.

The attributes of the various objects could be divided into two types: specification information and simulation information. Specification information is the design information that allows a spacecraft engineer to determine which components should be used in a particular design. Information of this type includes attributes such as peak power, mass, and operational temperature range. Specification information can be used when a simulation is being compiled, but it is typically not passed dynamically at run time. Simulation information includes the attributes and interactions of a component which are computed and updated during a simulation. This type of information includes parameters such as instantaneous power usage, momentum, and torque. These parameters, normally not used during the design phase, are important for simulating the effects that a component has on a larger system.

This ATD project began with an overall consideration of the virtual spacecraft. As work progressed, focus was provided by limiting the scope to the attitude control subsystem. At this time, a set of preliminary standards has been written for several of the components and is being used to realize an executable simulation. We have interacted with staff at the Jet Propulsion Laboratory and the Goddard Space Flight Center in carrying out this work. If industry-wide standards are to be developed, the industry must be widely involved. Collaborators, both government and commercial, must "buy into" the process. We feel that there is ample potential

benefit to make this happen. In the first place, there will be a market for standardized classes and objects, both for components and for environmental and physical glue objects. Second, there will be a need for developmental tools and environments that facilitate the simulation development process. And finally, there will be a market for training services: as the industry becomes standardized, companies will need to learn these standards if they are to be players in the growing spacecraft development enterprise.

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