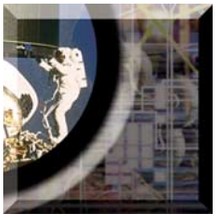

Microsatellites: An Enabling Technology for Government and Commercial Aerospace Applications

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The ongoing development of a three-axis stabilized microsatellite bus concept designed for critical, embedded government or commercial aerospace applications at APL is described. These microsatellites can form the basis for cost-effective, multiple *in situ* or remote sensing missions for monitoring physical phenomena; for missions enabled via flying a number of satellites in formation; and for a constellation of satellites launched by a low-cost launch vehicle. The foundation for this microsatellite bus concept, with a weight of 30 kg and size of 20 × 20 × 61 cm, is based on technologies and manufacturing processes now in place or being developed at APL. The microsatellite and its foundational technologies are being advanced for insertion into current and future APL Space Department proposals and programs and are also candidates for technology transfer to industry for commercial applications.

INTRODUCTION

This article describes APL's three-axis microsatellite ("microsat") bus concept and the enabling technologies under development at the Laboratory. Although the primary focus of our work is on spacecraft avionics, other enabling technologies being developed by APL in the areas of propulsion, sensors, and structural elements are also described. A chip-on-board (COB) miniaturization process has been developed and was used to implement microsatellite onboard electronics. The development of the Integrated Power Source (IPS) introduced a new dual-use independent power panel technology that can provide structural functionality as well. APL has collaborated with private industry, other universities, and government agencies for the development and procurement of actuators, power storage elements, etc., to complete the array of subsystem elements in an initiative to reduce costs. We have used a satellite altimetry mission, the Water Inclination Topography and Technology Experiment (WITTEX),[1] to create a consistent set of spacecraft requirements to verify that the technologies described can indeed make a revolutionary change in the approach to future missions. Our WITTEX conceptual design, which employs the technologies described in this article, shows that a mass reduction factor of 20 is achievable as compared to the TOPEX spacecraft, which had similar functional capabilities.[2]

A significant component in the end-to-end cost equation is attributable to the launch vehicles. The

difference between a vehicle that launches thousands of kilograms of payload (e.g., Delta 7925) and one that launches hundreds of kilograms of payload (e.g., Pegasus or Taurus) is about $30 million (Table 1). This represents an impressive savings and a compelling rationale for the development of microsatellites that can be launched either individually or as a constellation on a single low-cost launch vehicle.

A volumetric study determined that 10 microsats sized 31 cm in diameter and 92 cm high could fit within the fairing of the Pegasus vehicle; 20 microsats could be accommodated by the Taurus (Fig. 1). Thus, the cost-effective launching of instant constellations is now feasible. Consider, for example, the need for linking battlefield units and commanders with command headquarters. Instant constellations can potentially be launched to support the gathering and fusion of data for enhancing battlefield situational awareness. Other innovative missions enabled via microsatellite technology include formation flying, multiple *in situ* sensing, interferometric science, and mother-daughter spacecraft initiatives. Potential commercial sector applications include the use of microsatellite clusters and constellations for all types of communication; gathering and relaying of data for resource management, e.g., crops, ships, vehicles; emergency management, e.g., forest fire detection; and others yet to be conceived.

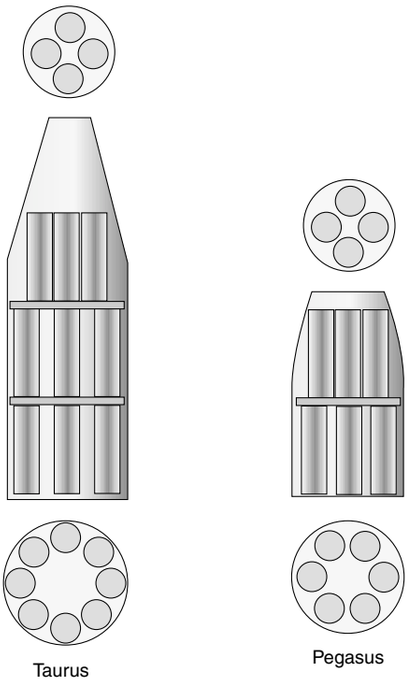


Figure 1. Microsat concept (volumetric study).

SYSTEMS APPROACH

Miniaturization of space systems involves factors beyond the usual requirements for small size and low mass. APL's systems approach considers the development of the microsatellite bus from an end-to-end perspective. The approach begins with top-down deliberations on the design of an electronics architecture suitable for miniaturizing all physical aspects of the microsatellite. This includes the use of highly integrated electronics technologies as well as the integration of functions classically implemented in separate elements with the IPS (see the article by Schwartz et al., this issue), which combines energy storage, solar array electronics, and charge control electronics into a single structural element. Sensors, actuators, and other structural elements needed for a specific mission must meet the small size and mass requirements and operate within the electronics architectures selected. In all of these systems the minimization of power facilitates overall mass reduction and is an important design parameter.

With a conventional satellite electronics architecture, functional electronics subsystems are connected with wiring harnesses distributed throughout the satellite, adding considerable weight and volume. Typically, the harness is about 7% of the dry spacecraft weight. With an integrated electronics module (IEM) approach, however, much of the onboard electronics are packaged onto electronics boards that are integrated into a single housing in which the boards are connected in a backplane fashion. This can result in considerable weight and volume savings. The Laboratory's IEM design integrates the IEEE 1394 backplane serial communications bus protocol, which has been implemented with efficient electronics that dissipate half an order of magnitude

Table 1. Launch vehicle costs.[3]

Vehicle	Payload weight (kg)	Launch cost ($M)
ARIANE 4 (auxiliary payload)	50	0.083
Pegasus XL	460	12
LLV-1	800	16
Conestoga 1620	889	19
Taurus	1400	19
LLV-2	1990	21
LLV-3	3655	25
Delta 7925	3990	48
AR40	4900	53
Atlas II	5510	80
AR44P	6900	88
SL-4	7000	19
Zenit-2	13740	40
AR5	18000	120
Proton D1	20900	60
Tital IV/SRM U	21640	222

less power (for 10 communication nodes) at 100 times the data bandwidth as compared with conventional 1553 technology (see the article by Fraeman, this issue). To minimize the physical implementation of the onboard power system and thermal system, this IEM design incorporates power-efficient electronics at the board level.

For power savings, the design of low-power electronics factors in power management techniques and considers low supply voltages. The power dissipated in CMOS integrated circuits (ICs) is a function of CV^2f, where C is the load capacitance, V is the supply voltage, and f is the clock frequency. While physics defines the power needed for the radio-frequency (RF) electronics, digital electronics power dissipation can be managed by carefully choosing the supply voltage and managing the clocking frequencies. Research in the development of ultra low power <1 V CMOS ICs suitable for space is encouraging and will likely result in major reductions in power dissipation in digital electronics. A recent study[4] showed that the use of ultra low voltage IC technology can yield a 20 to 50% saving in power, largely from a reduction of digital electronics power consumption. Part of the challenge of using <1 V IC technology is in supplying power at low voltages with high efficiency. APL has a low-voltage DC/DC converter design operating at nearly 80% efficiency at a 0.5 V output.

With a compact electronics architecture, the electronics must be designed to incorporate the fewest components on boards that can be integrated in the most compact format possible. At the component level, parts selection focuses on the integration of the smallest outline packaged parts (i.e., chip scale packaging) that are available for space use. Indeed, the smallest area required for the implementation of electronics involves mounting just the IC die itself and dispensing with the housing package for the die. This is the technology of COB packaging (see the article by Ling et al., this issue), which allows for mixing die and packaging parts on the same organic multilayered printed circuit board (PCB), since all parts are not available in die form and some parts are less expensive in packaged form. The ability to mix die and packaged parts is a critical attribute that makes COB cost-effective while reducing electronics with the same complexity by an order of magnitude. It is important to note that COB electronics are repairable, another cost-effective attribute, especially for government space programs. Thus, the development of microsatellites is enabled by APL-developed COB miniaturization packaging technologies.[5]

At the chip level, custom and semicustom ICs and field-programmable gate arrays can integrate many functions onto the fewest number of ICs to reduce the parts count in the implementation of the electronics. Fewer components enhance reliability as well as reduce weight and volume. Among other important aspects in the design and development of application-specific ICs, besides cost and schedule concerns, are the radiation tolerance of the design and its implementation on the selected IC foundry line. With just two IC foundries in the United States that can produce hardened ICs, the Laboratory is taking a complementary approach to develop radiation-hardened devices by design, versus acquiring parts from a "rad-hard" foundry supplier. With rad-hard parts, an APL microsatellite can be designed for critical applications for government, DoD, and commercial sponsors.

Taken together, these systems considerations, along with the technologies that are described in this article, form the basis for the development of a microsatellite bus that can be used for innovative missions which have not been cost-effective with yesterday's conventional satellite technologies.

THREE-AXIS STABILIZED MICROSATELLITE

A block diagram of the APL microsatellite bus is given in Fig. 2. The center portion delineates the functional single-string electronics in the form of individual cards that comprise the miniaturized IEM. The command and data handling (C&DH) processor, solid-state data recorders (SSRs), and spacecraft general-purpose processor slices which comprise the command and data handling in your palm (C&DHIYP) unit (discussed in detail later) form the basis for the microsatellite avionics.

Other miniaturized electronics slices in development at APL include low-power RF receiver electronics and Global Positioning System (GPS) navigation slices. The RF receiver slice will incorporate a scalable architecture that can be adapted for S- or X-band operation for near-Earth or deep space missions. The miniaturized GPS receiver design is based on the Thermosphere-Ionosphere-Mesosphere Energetics and Dynamics (TIMED) GPS receiver design (see the article by Chacos et al., this issue) and will include a feature for implementing cross-link transceiver functions designed for formation flying.[6] Electronics for power management, attitude control, thermal control, and instrument interfaces are not high-risk areas for the microsatellite and can be readily designed to meet the needs of any desired mission.

As noted earlier, all of the electronics in the IEM are connected via the high-speed IEEE 1394 protocol and a number of standard low-speed serial buses. These slices and other electronics design boards are integrated in the IEM with fuzz button connectors that form a *de facto* motherboard. Connections to other onboard electronics and instruments are via edge connectors on each electronics board. These advanced technologies collectively form the basis of a tightly integrated (both physically and electronically) electronics module of

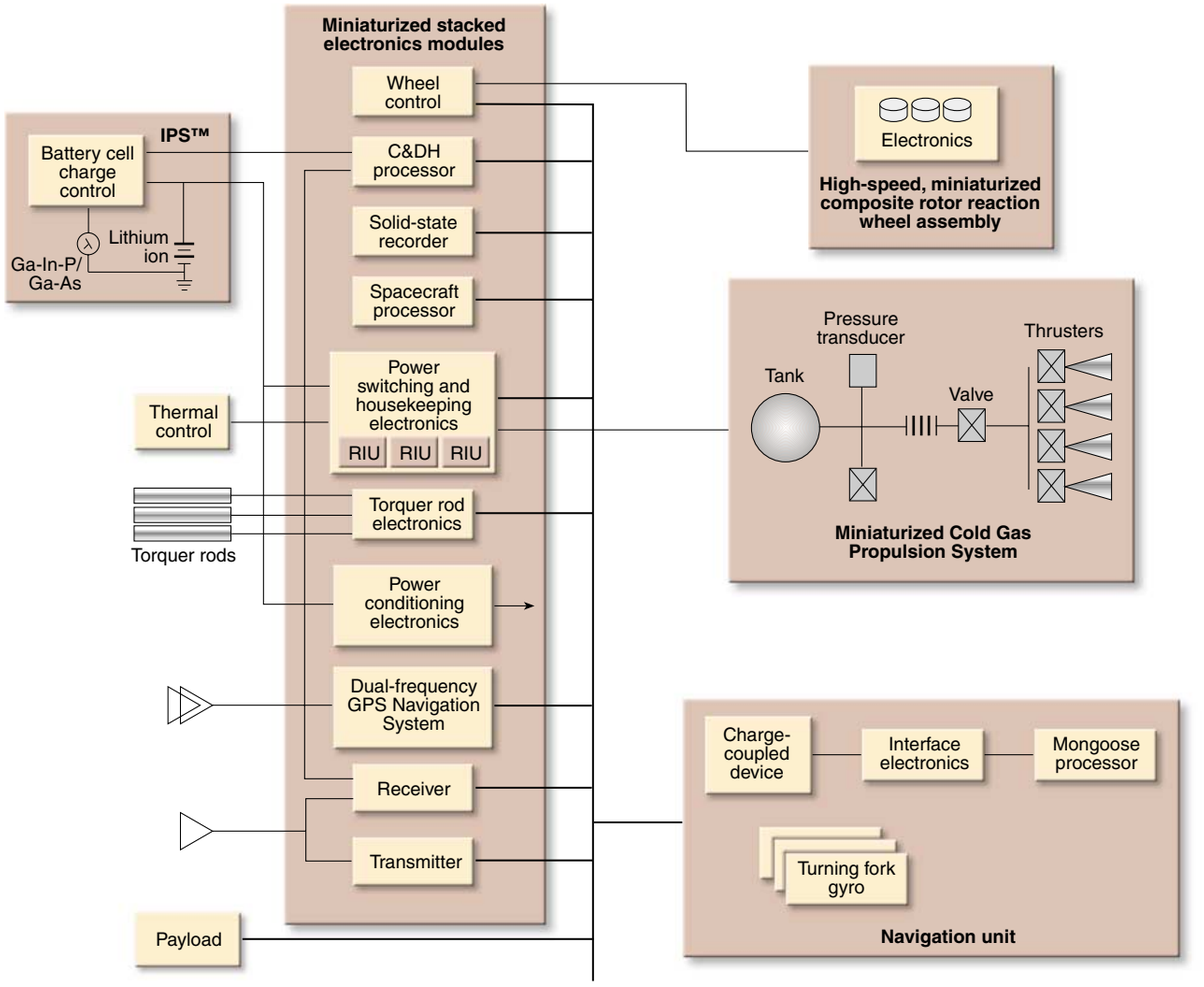


Figure 2. APL microsatellite bus block diagram (IPS, Patent #5,644,207; RIU = remote interface unit).

10 × 10 cm × the number of slices that can meet the infrastructure needs of a microsatellite.

The IPS—a new innovation that has been under development with NASA Advanced Technology Development funds—will allow a high degree of power management autonomy. A cold gas miniaturized propulsion system has been developed for ΔV maneuvers and station keeping. The IPS and cold gas system are discussed later in the technologies section.

The navigation unit will be developed with small-to-miniature commercial off-the-shelf (COTS) magnetometers, reaction wheels, gyros that are available from industry, and APL-developed sensors such as the micro digital solar attitude detector (μDSAD) chip that is currently being transferred to industry (see the article by Strohbehn et al., this issue). Leveraging on industry components will contribute to cost savings.[7]

The microsatellite bus is sized at 20 × 20 × 61 cm and has a 30-kg mass goal. The IPS power panels will be designed to be structurally suitable for use as side panels and can also be deployed for additional power generation. Minimizing the structural weight is important in the development of the microsatelllite. We have focused our effort on the design of a low-cost composite structure that uses simple geometry to minimize tooling costs (Fig. 3).

MICROSAT ENABLING TECHNOLOGIES

Miniaturization Technology

Miniaturization of space electronics requires an understanding of all aspects of packaging technology, from the bare die level to the systems level. Cost, performance, schedule, and reliability are the primary drivers in the electromechanical development of space electronics. The APL Space Department launched several

Figure 3. A composite model of the microsat bus.

internal research and development initiatives to address packaging technologies for the cost-effective miniaturization of electronics. Among the list of techniques available, such as multichip module (MCM), ball grid array, and flip chip, COB was selected for its advantages over the others.

COB technology directly attaches IC die and other packaged parts to organic PCBs, leveraging on well-known technology. Figure 4a shows the various sizes of IC die packaging types.[8] The flip chip is an unpackaged IC die with conductive bumps on the bottom to implement connections to the IC. The package-to-chip ratio is by definition 1:1 for the flip chip. Figure 4b depicts packaged parts on PCB and COB technology.[9] The IC dies show how area-inefficient dual-inline packaging is. The die carrier takes up most of the PCB. MCM techniques allow the chip to be directly attached to a substrate with a hermetically sealed covering. Rework with MCM technology is very difficult. COB technology directly attaches the die onto an organic multilayered PCB. Our tests show that there is no need to hermetically seal the entire board (Ref. 5; see also the article by Ling et at., this issue). Direct attachment of the die with surface-mount technology reduces thermal resistance for improved performance and minimizes interconnects.

COB technology can accommodate packaged parts as well as dies, a significant attribute since, as already noted, some parts are not available in die form and some parts are less costly in packaged form. With COB technology, all parts on the board are accessible and consequently repairable, a desirable asset in the low-volume research and development environment. The leveraging of standard printed wiring board and existing hybrid technology allows for cost-effective high-density packaging. COB clearly emerged as the leading technology for the implementation of APL's microsatellite technology. APL has developed a COB process that can produce spaceflight-qualified miniaturized electronics. Two miniaturized electronics systems are in development: a C&DH system and a miniaturized charge-coupled device visible imager.[10]

APL is continuing to develop advanced packaging technology to further miniaturize space electronics. With NASA support, flip chip technology and high-density substrates with micro via technology are being investigated. Flip chip technology can achieve smaller packaging size; better thermal, mechanical, and electrical performance; higher product reliability; and cost-effective manufacturing. Emerging interconnect technologies, such as anisotropic conductive adhesive with Au/Ni bumped dies, nonconductive paste with Au stud bumped dies, isotropic conductive paste with Au stud bumped dies, as well as conventional solder processes are being investigated (see Ling et al., this issue). Some of the advanced flip chip interconnect technologies are especially suitable for space applications where small quantity is commonplace. Bumps can be applied on individual bare dies for the flip chip process.

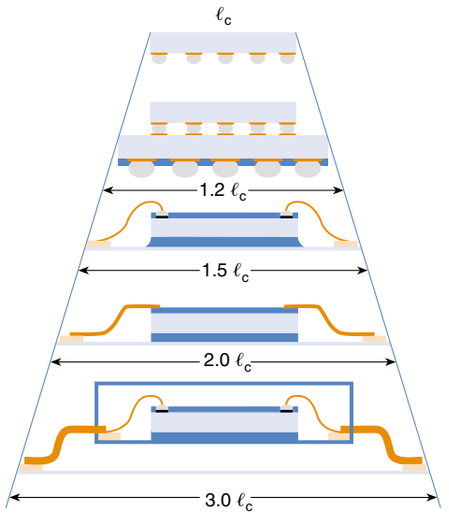
High-density substrates with micro via technology play an important role in electronic miniaturization. Components with ultra-high I/O density cannot be implemented without corresponding reduction in PCB feature sizes. High-density substrates can accommodate more parts for a given area, thus reducing the final system weight and volume. APL is developing ultra-high-density board designs for space applications employing very small feature sizes in line width and spacing (75 μm), together with blind (150 μm) and buried (250 μm) vias with high aspect ratios.

With COB and other miniaturization processes that are now in place or being developed, the miniaturization of space satellite buses and payload instruments and packages is now feasible to support innovative, cost-effective missions for the new millennium.

IEM

Traditionally, a satellite's electronics are organized in many functional subsystems, each housed in its own chassis. Chassis are heavy, take up considerable space, and are connected by cabling that constitutes an undesired fraction of the spacecraft weight. The IEM eliminates this drawback by collapsing most of the core spacecraft control electronics into a single chassis. All resources within the IEM are effectively cross-strapped. Fault tolerance is achieved by duplicating critical cards and switching to the redundant channel in

(a)



Technology	Area ratio: package/chip
Flip chip	1:1
Chip-scale package	1.5:1
Chip-on-board	2.25:1
Tape automated bonding	4.0:1
Quad-flat package	9.0:1

(b)

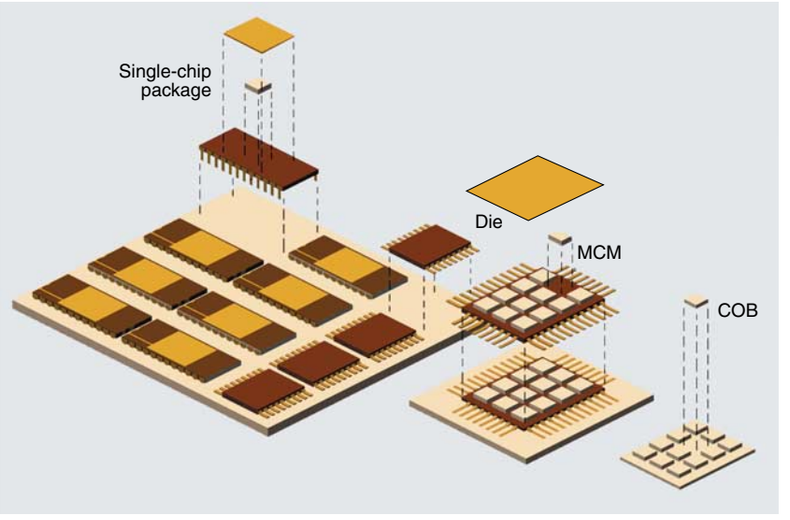


Figure 4. Die and packaged ICs: (a) comparison of several technologies (ℓ_c = length of chip side),[8] and (b) comparison of conventional and COB packaging.[9]

case of failure.[11] Subsystems communicate over the standardized, redundant IEEE 1394 high-speed, low-power serial bus within the IEM that supports up to 50 Mbits/s across the backplane (see the article by Fraeman, this issue).

IEEE 1394 is rapidly emerging as a significant standard and is gaining widespread support in the computing and digital video industries. APL has implemented the IEEE 1394 circuitry and is now seeking to port VHDL design, a very high-speed integrated circuit hardware description language, to an application-specific IC IEEE 1394 protocol chip that links each card within the IEM. Low-speed auxiliary digital serial buses for collecting status and engineering housekeeping data have been designed for the IEM (e.g., various industry-standard serial links based on RS-422, I^2C, and Mil-Std 1553). Information is collected where it is measured and digitally transmitted over a serial bus to the IEM. This methodology is flexible and can easily accommodate changes to the number and type of monitored parameters, even late in a spacecraft's design cycle. Subsystems are also designed to be readily reused on different missions, resulting in significant nonrecurring development cost savings.

When appropriate, an individual board design may also be upgraded without impact on other subsystems within the IEM. The functionality of the core board set is optimized across traditional spacecraft subsystem boundaries to improve power efficiency and reduce mass. Circuitry unique to specific missions can be included, and performance can be readily enhanced with additional general-purpose processors and task-specific circuits. Finally, the IEM architecture is designed for reusability, flexibility, modularity, scalability, and enhanceability. The resulting IEM single box implements communications, guidance, navigation, attitude control, power control, health and safety, and C&DH functions for the spacecraft.

C&DHIYP

With the compact IEM architecture and COB miniaturization technology, APL, under sponsorship from NASA Goddard Space Flight Center, developed C&DH functional slices to form the basis for the integrated electronics suite for this microsatellite bus.[12] This set of stackable electronics boards was designed and packaged to be small enough to fit into the palm of the hand (thus, command and data handling in your palm).

The C&DHIYP block diagram (Fig. 5) delineates four electronics boards: an embedded RTX2010 processor for C&DH functions (microcontroller module), an SSR module capable of storing 2 Gbits of data, an applications module (which could serve as a general-purpose onboard computer), and a power converter module. The electronics for each module are packaged onto a 10-cm^2

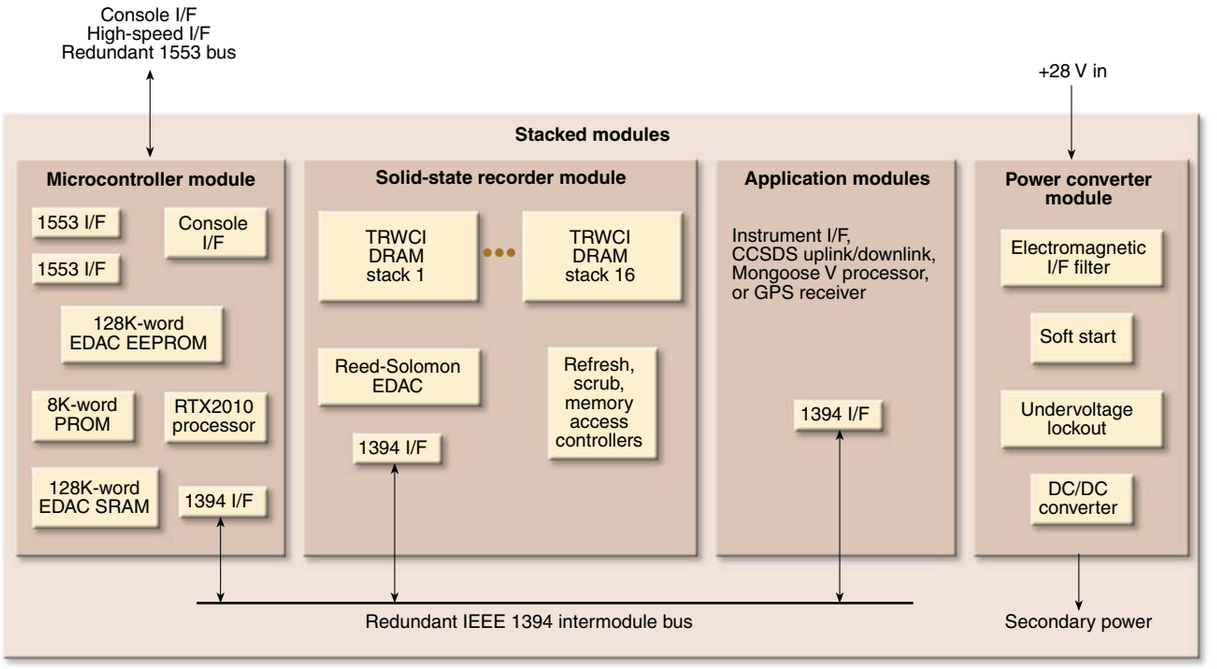


Figure 5. C&DHIYP block diagram (10 × 10 × 5 cm, 0.6 kg). (CCSDS = Consultative Committee for Space Data Systems, DRAM = dynamic access memory, EDAC = error detection and correction, EEPROM = electrically erasable PROM, EMI = electromagnetic interface, GPS = Global Positioning System, HSS = high-speed serial, I/F = interface, PROM = programmable read-only memory, SRAM = static random-access memory, TRWCI = TRW Components International.)

multilayered PCB that is individually housed in an aluminum frame that is designed to be stacked. The stackable fuzz button connectors form the electrical interconnections between the slices and therefore implement a *de facto* scalable motherboard that can extend as far as the number of modules in the stack. Each slice is about 1 cm thick and weighs about 105 g. The frame functions as a handling fixture during fabrication and test of an individual module and becomes part of the flight chassis as modules are stacked.

Three C&DHIYP modules are now in development: the RTX2010 processor and I/O module (Fig. 6), the SSR module, and a Mongoose V all-purpose processor and I/O module. The RTX2010 slice is a critical embedded processor design based on the FORTH language running at about 2 to 3 MIPS to handle the onboard C&DH and data collection functions designed for a microsatellite. This radiation-hardened microprocessor is also immune from bit upsets due to high-energy particles, thus making the design suitable for high-reliability critical embedded applications. It communicates with the other modules via the IEEE 1394 serial communications protocol and includes MIL-STD 1553 and high-speed serial interfaces to other electronics and instruments onboard the satellite. This slice dissipates 3 W.

The SSR module is designed for use as a bulk storage device for science, housekeeping, or any other onboard data. It uses stacked DRAMs to maximize capacity and Reed-Solomon block coding to minimize the error rate. For this particular design, the capacity is 2 Gbits, with a standby power of 1.8 W and operating power of 5.7 W.

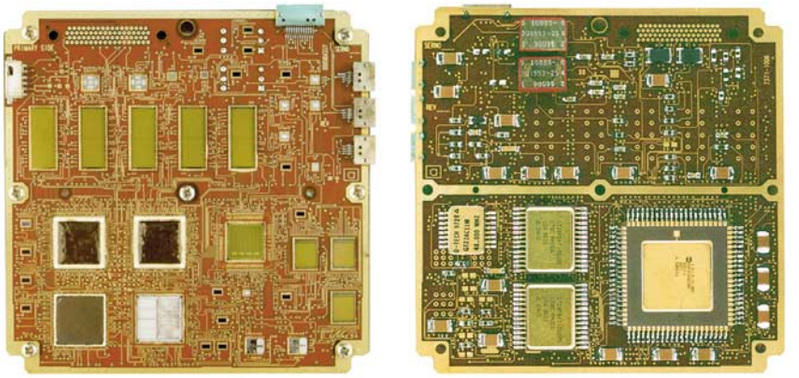


Figure 6. The front (left) and back (right) of the COB implementation of the RTX2010 processor board (size = 10 cm^2).

With current stacked DRAM technology, this board could be designed to store 20 Gbits of data.

The Mongoose V module is designed to be a high-performance computing element. Again, the IEEE 1394 protocol is used for board-to-board communications. The Mongoose design incorporates 2 Mbytes of RAM, 5 Mbytes of EEPROM, 32 Kbytes of boot PROM, as well as 16 Mbytes of DRAM.

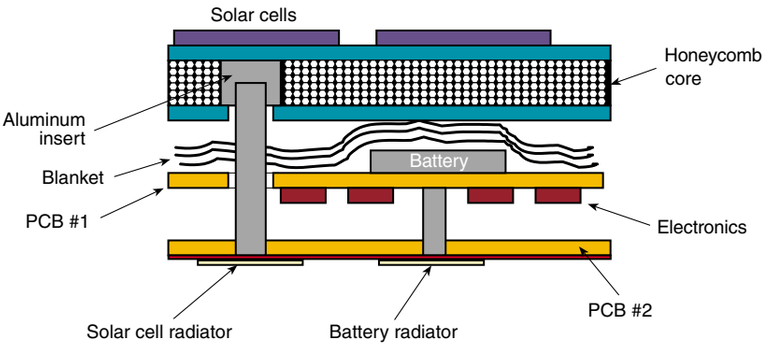


Figure 7. The first-generation IPS.

Microsat Power Systems and the IPS

Traditional spacecraft power systems that typically require some level of ground management incorporate a solar array energy source, an energy storage element (battery), and battery charge control and bus voltage regulation electronics to provide continuous electrical power for spacecraft systems and instruments. Dedicated power converters condition power for individual loads and provide limited fault isolation between systems and instruments, while a centralized power-switching unit provides spacecraft load control. Protection of the spacecraft battery from undervoltage conditions that can result in battery cell failure typically depends on hardware fault detection to alert the spacecraft processor, which removes fault conditions and noncritical loads before permanent battery damage can occur.

The cost-effective operation of a microsat constellation requires a fault-tolerant spacecraft architecture that minimizes the need for ground station intervention by permitting autonomous reconfiguration in response to unexpected fault conditions. APL has developed a new microsat power system architecture that enhances spacecraft fault tolerance and improves power system survivability by continuously managing the battery charge and discharge processes on a cell-by-cell basis. This architecture is based on the recently patented IPS, which integrates solar cells, an energy storage layer, and processor-based charge control electronics into a structural panel that can be deployed or used to form a portion of the outer shell of a microspacecraft.

The first-generation IPS is configured as a 2.5-cm-thick panel in which prismatic lithium ion battery cells are arranged in a 3×7 matrix to provide 26 VDC and a 5×1 matrix for 3.7 VDC output voltages (Fig. 7). The battery cells on the energy storage layer are insulated with a thermal-blanket insulating layer to protect the lithium ion battery cells from the extreme temperatures of the solar cell layer. Thermal radiators, located on the back of the panel, are dedicated to the solar cell layer and the battery cells. In deployed panel applications, these radiators maintain the battery cells in an appropriate operational temperature range. In body-mounted panel applications, solar array and battery heat is independently routed to remote radiators.

The IPS electronics sense the instantaneous charge current, cell voltage, and temperature of each battery cell to control the charging process and maintain charge-state equality among all battery cells in the matrix. The electronics include a processor that sets the charge current for each string of cells in the battery matrix, controls individual cell bypass currents to implement the control algorithms, and maintains charge-state equilibrium in the absence of precisely matched battery cell characteristics. The charge control processor can be programmed to permit the use of virtually any flight-qualified battery chemistry, and can recognize and correct battery cell conditions that may lead to cell failure or reduced cell life. This feature allows for graceful degradation of the power panel in the event of anomalies. The processor continuously generates a coulometric record for each battery cell, which provides critical information for spacecraft energy-balance–based autonomous control algorithms, yielding a very accurate fuel gauge. Patent #6,157,167 for the control electronics has recently been granted.

The microsat power system architecture provides unregulated voltages that can be distributed to spacecraft systems and instruments in a traditional manner or used to power dedicated spacecraft loads through linear regulators or power converters. Critical and noncritical spacecraft loads can be powered from independent power sources, further improving spacecraft fault tolerance and reducing microsat constellation operational costs. In addition, eliminating the shared power lines among spacecraft systems and instruments eliminates the conducted power line noise coupling that is typical of traditional architectures. Spacecraft integration testing can be simplified by eliminating portions of the traditional battery of integration tests.

Microsatellite Propulsion System

The Cold Gas Propulsion System (CGPS; Fig. 8)[13] that has been designed for microsatellites addresses

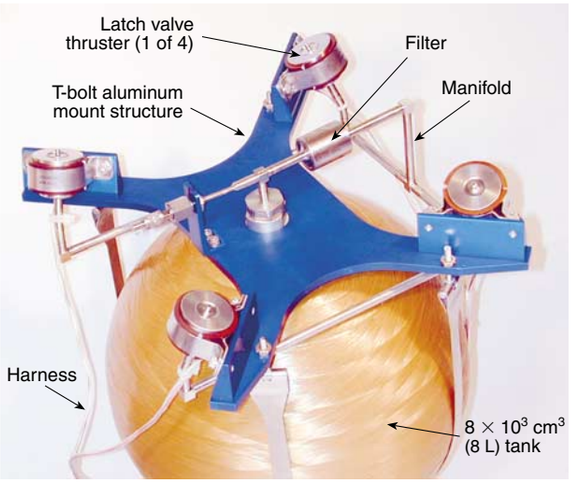


Figure 8. The Cold Gas Propulsion System.

major design drivers for low cost, minimum power/mass, small envelope, and simple architecture. The requirements for this design were based on a strawman mission for a constellation of microsatellites launched into multiple planes of a 700-km orbit inclined 63°, with each plane populated by the single launch of six to eight microsats. The required ΔV is a function of the duration allowed to accomplish drifting as well as how far the spacecraft is required to drift around the orbit. It is assumed that there are 30 days available for drifting, and the drift distance is the maximum or 180°. This results in a constellation establishment ΔV requirement of 30 m/s.

Maintaining the desired spacing between each spacecraft during the mission lifetime requires additional ΔV. For the assumed 5-year mission lifetime, this results in a 20-m/s requirement, for a total of 50 m/s for each microsatellite. The CGPS uses a simple "blow-down" architecture that requires the entire system to operate at full storage tank pressure, thus eliminating the traditional pressure regulator. This called for the development of unique thrusters capable of functioning with inlet pressures up to 200 bar (3000 psi).

Nitrogen gas is used for this prototype microsatellite propulsion system. The tank is a COTS spherical aluminum shell tank with a Kevlar filament overwrap. The thrusters use a latching valve design that requires a pulse to open and a pulse to close. Between pulses the thruster is magnetically latched in either the open or closed position as required. This dramatically reduces the power needed by the thruster valves while preserving the option for small impulse bits. To minimize cost and mass, the system uses only four thrusters. By mounting these thrusters in a double-canted orientation to the spacecraft, pitch, yaw, and roll control as well as ΔV can be accomplished.

TECHNOLOGY INSERTION

The microsatellites described here can form the basis for new missions involving multiple satellites and swarms or constellations of satellites. Formation flying is of high interest to many sponsors. For example,

- The Air Force is studying the development of multiple satellites flying in a tightly coupled formation to implement a sparse aperture to achieve performance equivalent to a physically large antenna aperture for radar applications in the TECHSAT Program.[14]
- Programs with multiple satellites flying in loose formation are enabling a new class for three-dimensional viewing and analysis of scientific phenomena with stereoscopic or multiscopic *in situ* or remote sensing. The Solar Terrestrial Relations Observatory (STEREO) mission[15] currently being developed at APL will image and explore coronal mass ejections (CME) from the Sun from two spacecraft to provide new perspectives on the consequences of CME interactions with the Earth.

These loosely or tightly coupled microsatellite missions enable time/space science studies of terrestrial and space phenomena.

The WITTEX concept mentioned in the Introduction involves two to three microsatellites, each with its respective delayed Doppler radar launched in the same orbital plane with specific orbital phasing to study the littoral region in a time-sequenced manner. This approach was not previously practical, since costly conventional-sized satellites require large launch vehicles. Multiple satellites exploring signals from the same physical phenomenon can be designed for interferometric science and analysis to yield additional insights. Instant constellations launched from a single low-cost vehicle, for example for DoD communications purposes, can be decisive in times of conflict, especially when the conflict disables in-place satellite assets. These representative missions are just a sampling of new missions that are enabled by microsatellites.

CONCLUSION

Advanced technology initiatives at APL have contributed to the development of a microsatellite bus design suitable for high-reliability critical embedded applications. Current innovations include a robust and modular spacecraft bus architecture, an autonomous IPS panel, and highly integrated custom electronics. Together with our COB process, these technologies are the basis for the design and implementation of microsatellites that can be cost-effectively launched individually, in clusters, or in constellations via low-cost launch vehicles. The realization of this capability will enable and expand the spectrum of new and innovative missions that include satellites flying in loose or tight

coupling for all sorts of commercial, civil, and DoD applications.

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ACKNOWLEDGMENTS: The authors gratefully acknowledge H. K. Charles Jr., T. C. Magee, and P. D. Wienhold of the Technical Services Department; J. F. Bogdanski, W. E. Radford, D. F. Persons, T. M. Betenbaugh, B. D. Williams, and D. S. Mehoke of the Space Department for their valuable contributions during the development of the microsat bus; and G. H. Fountain, R. K. Raney, D. L. Porter, and J. R. Jensen for the WITTEX conceptual application.

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