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COMPUTING AT APL MOVES INTO THE NINETIES

Being in the right place at the right time is always a great feeling, and my job at APL has been no exception to this. It has been my privilege to have worked my entire career in what must surely be the most rapidly developing technology in the history of mankind. It has been an exciting ride, and as Al Jolson used to say, "Folks, you ain't seen nothin' yet." The next 25 years will be even more exciting.

The Applied Physics Laboratory has been in the thick of it, and the past 25 years have brought great changes in the computing activities of its staff. My colleagues and I find ourselves smiling and shaking our heads in disbelief when we reminisce about the methodologies we were using only four or five years ago. The theme of this issue of the *Technical Digest* is a snapshot of APL's ever-changing computer activities as we approach the 1990s.

The difference between APL's computing environment the day I started and now can be well characterized by a personal anecdote. While being interviewed by the APL recruiter, I asked about the computing resources available here. He replied proudly that they consisted of an IBM-7094 central mainframe. If a recruiter were asked that question today, he would have to rattle off a list that included the following:

1. Several dozen VAX's and other minicomputers equipped with backend array processors.
2. A sizable number of Apollos, SUN's, and other computer-aided design workstations.
3. A wide variety of programmable Hewlett–Packard test equipment, including very large scale integrated (VLSI) testers and network analyzers.
4. Direct dial-up support to a remote Cray vector processor and to a Connection Machine.
5. Several image-processing and expert system workstations.
6. A unique special-purpose multiprocessor facility for processing huge amounts of wideband recorded sonar data.
7. A new QUEN memory-linked, wavefront array multiprocessor system invented at APL.
8. An experimental array of transputers for advanced radar signal processing.
9. Uncountable numbers of embedded microprocessor systems of a wide variety, including a Laboratory-developed VLSI Forth engine of the new RISC-class architecture.
10. Over 1000 personal computers for the technical and administrative staff that are directly linked in various local area networks and that have access to department and Laboratory-wide Ethernets.
11. A central mainframe facility.

This list describes a computing environment, wonderfully diverse and distributed throughout APL, the individual elements of which are tuned to specific applications. It never ceases to amaze me that most of those 1000 personal computers mentioned above have roughly the computing power of the old IBM-7094 mainframe.

The theme articles in this issue cover many of the items in the list. The first three, by Kenneth W. Koontz, Quentin E. Dolecek, and J. Robert Buchanan, have a common element: parallel multiprocessor systems. The article by Koontz discusses the problem of mapping a radar signal-processing task onto a transputer array (item 8); it is also a good tutorial on parallel processing. Dolecek writes about the QUEN (item 7), the multiprocessor system he invented, which is based on an architecture known as a wavefront array. Buchanan describes the architecture and applications of the Connection Machine (item 4), a new commercial system with 65,000 processing elements.

The fourth article, by Susan C. Lee and John R. Hayes, is especially interesting to me. It is about a development that culminates an APL program in custom VLSI, started in the early eighties, in which I have been an active participant. It is good to see seeds that you have helped to sow bear fruit. The fruit here is the SC32 (item 9), a language-directed, 32-bit microprocessor with an architecture based on the new Reduced Instructure Set Computer (RISC) concept that emerged in the mid-eighties.

In the midst of the computing explosion, a serious question for APL has been: How can the Navy best use the available computer technology in their tactical systems? This question is addressed by James G. Palmer in the fifth article. He examines candidate architectures for embedded applications to Navy systems and discusses the factors that control options and performance.

The next two articles offer examples of applications of the computing technology at APL. Lora L. Suther reviews the processing of spacecraft scientific data from instruments monitoring the Earth and solar system environment. She traces the history of the processing and

display techniques used at APL, showing the evolution as computational capability has grown. A. V. Louis Biggie, William E. Buchanan, Paul L. Hazan, and Alexander Kossiakoff describe a special software tool they have developed for rapidly creating and prototyping Computer-Assisted Instruction (CAI) software for children with learning disabilities. This tool makes use of the new Macintosh HyperCard technology.

The last two theme articles exemplify APL work in the new neural-network technology. The article by Vincent G. Sigillito presents some of the ongoing work in the Laboratory's Milton E. Eisenhower Research Center. He gives some very interesting results on the pattern-retrieval capability and storage capacity of neural-network associative memory architectures. The last theme article, by Sigillito, Simon P. Wing, Larrie V. Hutton, and Kile B. Baker, describes the application of a feedforward network to a radar classification task. The results are strong evidence of the power of this technique in signal processing.

These last two articles make a fitting lead-in to the nineties because neural networks are a wave of the future. I expect to see silicon analog neural-network processing chips emerge in the next decade as the building blocks of new computing machines.

THE AUTHOR

ROBERT E. JENKINS was born in Baltimore and received an M.S. degree in physics from the University of Maryland in 1965. He joined APL in 1961 and is supervisor of the Computer Science and Technology Group, an elected member of the APL Advisory Board, a member of APL's standing Independent Research and Development Committee, the program manager for Space Department Independent Research and Development, a member of the Electrical Engineering Program Committee for The Johns Hopkins G. W. C. Whiting School of Engineering, and a lecturer in electrical engieering at both the Homewood Campus and the APL education center. During 1978, Mr. Jenkins was visiting scientist at the Defense Mapping Agency. In 1985, he was awarded the Dunning professorship at the Homewood Campus, where he introduced a new course in very-large-scale integration design and conducted research in cellular automaton processing.