

TOWARD VERY LARGE SCALE INTEGRATION APPLICATIONS IN SPACE

An integrated circuit design facility has been established at APL to help tap the vast potential of very large scale integrated circuits for space applications. A custom N-channel metal-oxide semiconductor chip containing 7000 transistors has been successfully fabricated by a silicon foundry using the design database produced by the APL facility. This project is a tangible step toward creating a capability that could produce innovative and otherwise unavailable solutions to spacecraft systems problems.

INTRODUCTION

A promising new technology is the design of custom very large scale integration (VLSI) circuits. By "custom" circuits is meant unique monolithic chips, with limited and quite specific applications, produced in relatively small quantities. These integrated circuits (ICs) would have from 64,000 to 1,280,000 active devices apiece and give system designers unprecedented freedom to explore new solutions to systems problems. One objective is to establish at APL a capability for custom VLSI design, with a view toward innovative applications of this technology in spacecraft system architectures of the future. A very specific long-term objective is the capability by 1992 of designing spaceborne supercomputers that have the proficiency of a Cray-1 computer. Significant progress toward these objectives has been made.

APPLICATIONS

Space applications for VLSI technology abound. Powerful spaceborne computers and signal processors will be needed over the next decade for a wide spectrum of applications. Among these are

- Autonomous satellite self-navigation
- Spaceborne real-time image processing
- Signal processing
 - Filters
 - Frequency-domain transforms
 - Correlators
 - Convolution
- Array processing, matrix algebra
- Highly parallel computing
- Spacecraft autonomy
 - Intelligent communications
 - Automatic sensor calibration
 - Redundancy, fault tolerance, self diagnosis
 - Image construction, pattern recognition

Spinoff applications will include satellite ground support equipment and implantable biomedical devices. Features that make VLSI technology attractive for these applications are high density; low volume,

GLOSSARY OF ACRONYMS

CAD—Computer-aided design
CMOS—Complementary metal-oxide semiconductor
IC—Integrated circuit
NMOS—N-channel metal-oxide semiconductor
VLSI—Very large scale integration

weight, and power; and the ability to process expeditiously large amounts of data.

A number of very specific applications for VLSI have been identified. One is a programmable spectrum accumulator that serves as a preprocessor for data from spaceborne sensors. A complete 256-bin spectrum accumulator can be built by means of complementary metal-oxide semiconductor (CMOS) technology using 320,000 transistors. By the end of 1984, a 16-bin spectrum accumulator will have been achieved on a single monolithic integrated circuit. Spectrum accumulators are frequently used in energetic particle detection experiments to categorize particle types. A microprocessor in an experiment on a spacecraft can examine spectra and transmit to the ground only those data that are most interesting.

Another special-purpose preprocessing function for which VLSI is attractive is data compression. Because spacecraft telemetry bandwidth is often limited, a programmable data compressor such as a logarithmic compressor is frequently useful. A versatile logarithmic data compressor can be fabricated in CMOS using only 72,000 transistors. It is faster and more reliable to perform this function in a single VLSI circuit than to dedicate, say, half the resources of a microprocessor to it.

VLSI opens the door to many new applications that previously required too much weight, volume, or power to be practical in space. In spaceborne radar altimeters, for example, a high-speed digital "chirp" generator can be fabricated in a 3-micrometer silicon gate CMOS using only 56,000 transistors. In spaceborne image processors, 16 real-time cellular logic operations

can be performed on a 256×256 pixel binary image using one VLSI circuit containing 320,000 transistors.

Another advantage of VLSI is its ability to provide unique interfaces to spacecraft sensors and subsystems. With VLSI, a 12-bit successive approximation analog-to-digital converter requires only 10,000 square mils (0.01 square inch) of silicon area. This means that the converter can share the same VLSI chip with a data processing function. A video speed ("flash") analog-to-digital converter can also share a VLSI chip with a data processing function. VLSI, therefore, has great potential to solve applications problems that require intelligent sensors.

METHODS

There are many potential methods of using VLSI technology in such applications. One obvious method is to use the large families of new microprocessors and memory chips that are continually becoming available from commercial vendors. This is already being done extensively in APL-designed systems. Another potential method is to use the various processing chips (e.g., multiply-accumulators and fast Fourier transformers) now being developed by commercial vendors under the DoD Very High Speed Integrated Circuits Program. Many of the applications mentioned previously will come to fruition through microprocessor networks and hybridization of signal processing chips produced under the DoD program and commercially.

Chips can be designed to meet specific applications using semicustom design as a resource. Semicustom ICs include gate arrays, macrocell arrays, and standard cell arrays. These arrays are chips containing arrangements of standardized gates and cells that can be interconnected or "programmed" at the metallization layer. Gate arrays with several thousand gates are currently being used in several APL programs.

In general, however, systems design is probably more constrained than enhanced by the availability of off-the-shelf components, and the applications of VLSI will be affected by the components and resources made available by industry. This will be particularly true in space applications, for which radiation hardness is frequently necessary. An interesting aspect of VLSI is its potential for extending the designer's scope of control down to the device level through full custom chip design. This creates unprecedented opportunities in applications.¹

Highly parallel computing using arrays of microprocessors is an obvious and exciting prospect for many applications; however, for a limited class of problems, it may not be the best approach. We may frequently find ourselves trading a hardware design effort for an equivalent software design effort, with the price being a reduction in overall processing bandwidth. If custom design is truly practical, there will always be some systems where hard-wired processing logic is a better choice. Innovative applications will grow out of the creativity of the individual designers. The sharing of portions of a chip design may become as prevalent as sharing subroutines and programs

among software designers is now. Because of this high potential payoff, custom design was pursued in parallel with other VLSI methods, through a series of selected chip projects.

DESIGN TOOLS

To gain access to VLSI technology at the custom level, four primary questions have to be answered:

1. How does an engineer create a design for a custom IC?
2. How can the design be proven correct?
3. How does a government laboratory without in-house IC fabrication capability obtain prototypes or production parts of a custom design?
4. How can the finished ICs be tested?

To date, answers to all but the fourth question have been found and reduced to practice.

A custom IC design facility has been established at APL in response to the first two questions above. This facility is an integrated collection of powerful computer-aided design (CAD) tools, capable of supporting the design of chips containing more than 100,000 transistors. The various software tools were obtained from the University of California at Berkeley, from the Massachusetts Institute of Technology, and from Carnegie-Mellon University. Following are the most significant tools:

1. A hierarchical, interactive color graphics editor by which a design may be built from the mask layout level (the level at which actual fabrication masks are designed) on up to the complete IC level. The editor maintains a cell library of frequently used subfunctions, thus facilitating hierarchical design of the circuit. It maintains and manages the database that describes the design at the mask layout level.
2. A conversion program that can translate the editor database into Caltech Intermediate Form, a university-standard database format that is accepted by many silicon foundries and IC mask manufacturers.
3. A circuit extractor that can analyze the layout database, create a device and network description, and provide estimates of parasitic resistances and capacitances for the circuit.
4. Conversion programs that can translate the output from the circuit extractor into formats compatible with the logic simulator and circuit simulator.
5. A logic simulator that can perform functional verification of the design and can estimate circuit timing, potential race conditions, propagation delays, and so on.
6. A design rules checker that can verify proper adherence to layout design rules.
7. A detailed circuit simulator that can simulate actual node voltages and currents by modeling nonlinear devices and parasitic parameters. The simulator must include active device models that

are carefully matched to the fabrication process technology to be used. Accurate models and model parameters have been obtained for N-channel metal-oxide semiconductor (NMOS) and CMOS process technologies. All the design tools can be adapted to work with other process technologies.

All of these CAD tools are made compatible by maintaining data files in predefined formats. The file directory maintenance is performed by the UNIX operating system under which all of the tools run. The CAD tool set resides on a DEC VAX-11/780 superminicomputer but is easily accommodated on other computers with similar operating systems and comparable capability. The graphics editor requires a high-resolution color graphics terminal and a bit pad with mouse. Otherwise, all software can be accessed from an inexpensive "dumb" terminal.

FOUNDRY INTERFACE

The answer to the third question under "Design Tools," above, is that the government laboratory must go to a silicon foundry, a company that will cast layout databases into silicon wafers and provide packaging and test services. The difficulties in interfacing with a silicon foundry stem primarily from ignorance of the foundry language. Specifying masks for a complex IC is difficult at best, and the lack of standards for such specification makes it even more so. Different foundries use different terms to describe similar things, accept different database formats, require different kinds of working plates, and so on.

To address this difficulty, APL has subscribed to a multiple-source silicon foundry system that provides standards for design rules, circuit simulator model parameters, test cells, alignment marks, critical dimension marks, fiducial marks, mask specifications, etc. Participating silicon foundries agree to abide by these standards, so that a design created according to the multiple-source rules can be fabricated successfully at any of them. This multiple-sourcing for foundry services means that APL is not tied to a particular silicon foundry when the time comes to obtain prototype or production parts.

CHIP DESIGN

To prove that the design tools and foundry interface actually work, an NMOS integrated circuit was designed, simulated, and fabricated successfully. The goal of the design was to include on the chip major portions of the carrier tracking logic in a global positioning system navigation receiver.

The most recent designs for global positioning system receivers use a microprocessor to control the carrier and code tracking logic. The microprocessor performs arithmetic associated with scaling, integrating, and filtering the detected phase error signal. It then controls a digitally controlled oscillator, which is usually a form of binary rate multiplier.

The minimum required hardware functions for carrier tracking in this type of design are two identical phase error detectors/integrators, one for each quadrature component of the local digitally controlled oscillator, a binary rate multiplier to function as the digitally controlled oscillator, and some dividing logic at the output of the binary rate multiplier to generate the two quadrature phases of the local signal at baseband frequency.

To reduce the overall scope of the chip design to a realistic level, it was decided not to implement a complete stand-alone carrier tracking loop but to include the major pieces with enough input/output capability to test functionality. If, for demonstration purposes, it later proved desirable to include the chip in a breadboard version of an actual carrier tracking loop, the input/output structure of the chip would be adequate. Included were an 18-bit binary rate multiplier designed to operate at a clock frequency of 2.5 megahertz (MHz) and a phase error detector/integrator designed to operate at a sampling frequency of at least 10 MHz. Figure 1 is a block diagram of a microprocessor-controlled carrier tracking loop. The tinted area indicates the region that was included on the chip.

Two copies of the phase error detector, sine and cosine, would be required in an operational receiver; however, only one was included on the chip. This permitted the scope of the project to be expanded to include a switch to control the switching of a computer terminal between two terminal control units, and an expandable, parallel two's complement arithmetic multiplier design with wide application in signal processing. In addition, a number of test cells were included to gain experience in wafer probe testing and to evaluate the circuit simulation capability. Figure 2 shows the completed chip.

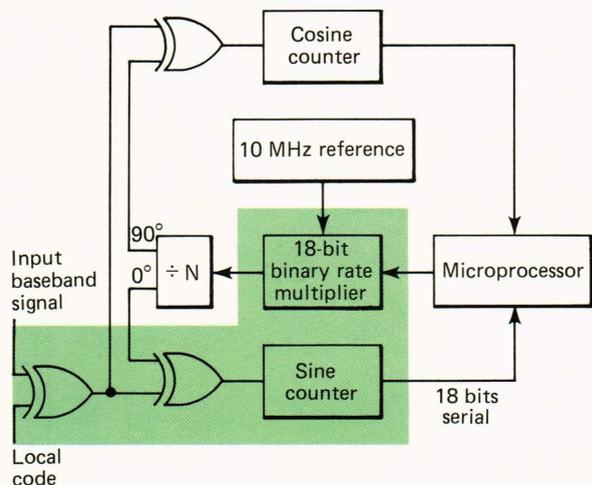


Figure 1 — Block diagram of a microprocessor-controlled carrier tracking loop in the digital portion of a global positioning system navigation receiver. The NMOS chip project (tinted region) includes an 18-bit binary rate multiplier, a phase comparator, and an 18-bit phase error integrator (sine counter). The binary rate multiplier contains 2320 transistors, and the phase comparator and error integrator contain 2732 transistors.

The graphics editor was used to create designs for a number of functional cells, the 10 major ones being

1. A toggle flip-flop used as high-order bits in the phase error integrator counters and in several divider circuits;
2. A D-type flip-flop, with asynchronous set and reset, that was widely used in various control circuits and in the control unit switch function;
3. A generator of two-phase, nonoverlapping clock pulses with superbuffer output line drivers;
4. An exclusive NOR gate with 20 nanosecond propagation delay that was used as a high-speed phase comparator;
5. A high-speed UP/NO-OP counter used as the low-order (least significant) bit in the phase error integrator counters and divider chains;
6. A compact binary full adder that was used in computing the effective up/down count in the phase error integrator;
7. A parallel-load, serial-shift register element to sample and shift out the phase error integrator results;
8. A clock synchronizer with a superbuffer output line driver, used in control sections to synchronize control signals with desired clock phases;

9. A two-bit counter module with synchronous carry propagation. Nine counter modules implement an 18-bit binary rate multiplier;
10. An output logic module for the binary rate multiplier that uses the positive edges of the counter outputs to produce a rate-controlled output.

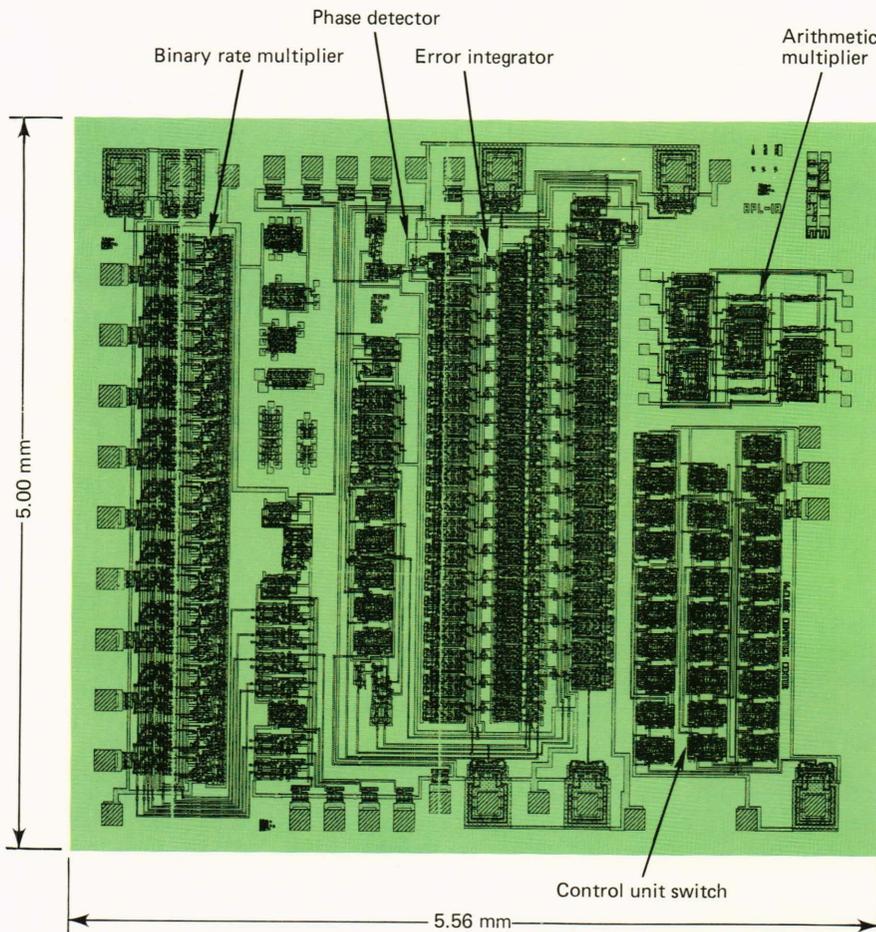
Figure 3 is a color-coded layout of a binary full adder. The layout for an output pad driver is shown in Fig. 4. The output pad is driven by a totem-pole configuration in which the large driver transistors surround the pad concentrically.

Figure 5, the finished design, is a photograph of the 200X magnification blowback films that were used to verify that the masks and working plates conformed in every detail to the original database. The foundry's color code was used in Fig. 5; orange represents diffusion and green represents polysilicon.

RESULTS

Ten processed wafers, each containing about 165 potentially good dice (unpacked silicon chips), were received from the silicon foundry seven weeks after the purchase contract was issued. The cost of the prototype run, including 25 packaged chips, masks, and working plates, was \$16,000. Figure 6 shows a finished wafer. The foundry was supplied with a detailed chip specification and the Caltech Intermediate Form tape

Figure 2 — Floor plan of the completed NMOS integrated circuit chip. Major subfunctions are called out. The binary rate multiplier requires 0.082 cm², the phase detector and phase error integrator require 0.099 cm², and the control unit switch and arithmetic multiplier require 0.069 cm². The process technology is 6-micrometer silicon-gate depletion-load NMOS.



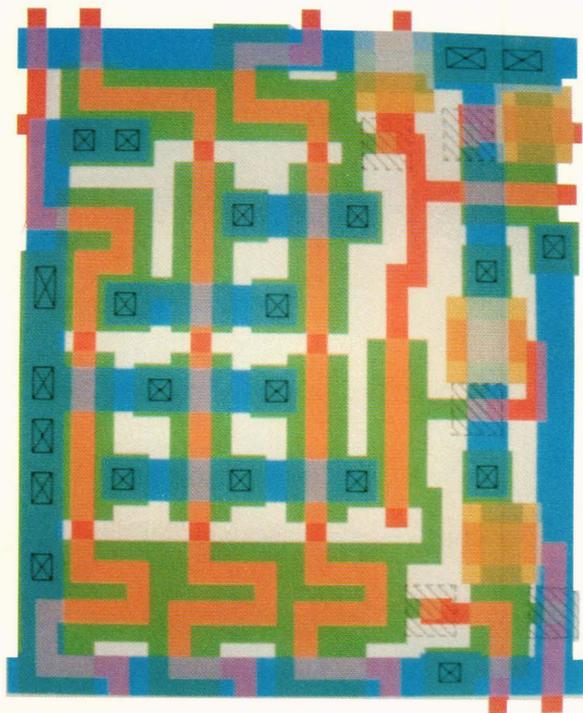


Figure 3 — A color-coded layout of a binary full adder. Green regions represent the N+ diffusion used to create transistor sources and drains. Red regions represent polysilicon, which is used for interconnections and to create transistor gates. (Wherever red crosses green, an MOS transistor is formed.) Yellow regions represent an ion implantation step by which normally-ON depletion-mode transistors are created. Blue regions represent aluminum metallization, which is used for interconnections and power distribution. Brown regions represent buried contacts connecting polysilicon to diffusion. Black regions represent contact cuts connecting aluminum to polysilicon or diffusion. This cell is 174 micrometers wide and 206 micrometers high. When N identical cells are abutted, the power supply rails and carry-propagation paths are connected to form an N-bit ripple-carry full adder.

output of the CAD system. Probe testing of the wafers and subsequent testing of the packaged chips (Fig. 7) verified that the circuits worked exactly as predicted by the computer design models. Pulses as short in duration as 20 nanoseconds were modeled accurately by the circuit simulator. The binary rate multiplier easily ran at 2.5 MHz, and the phase error integrator ran at clock rates up to 20 MHz. The completed circuits met all of their specifications and had comfortable speed margins.

The chip was 5.00 × 5.56 millimeters and contained approximately 7000 transistors. The technology was 6 micrometer NMOS, depletion load, silicon gate. The 2.5 MHz binary rate multiplier occupied 30% of the chip; the 20 MHz phase error detectors/integrator occupied 35% of the chip; the 5-MHz control unit switch and arithmetic multiplier occupied 25% of the chip; and test cells occupied the remaining 10%. So a figure of merit for this design is 1.2×10^{11} gate-hertz per square centimeter (see Table 1). This figure of merit is less than a factor of five below the phase 1 goal

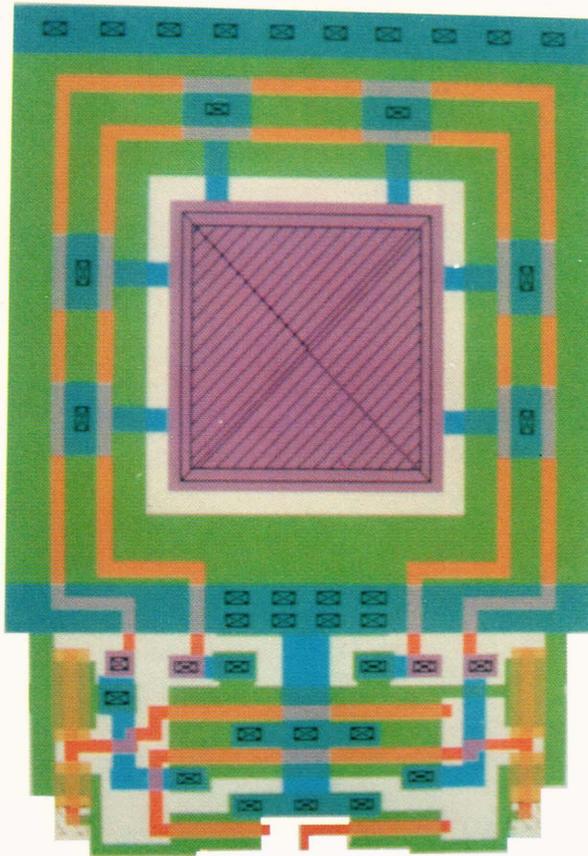


Figure 4 — A color-coded layout of an output pad driver cell. The two large pad driver transistors surround the pad concentrically. The pad is a region where wire bonds are made to connect the circuit to its package pins.

Table 1 — NMOS chip performance.

<i>Function</i>	<i>Gates</i>	<i>Maximum Speed (MHz)</i>	<i>Area (cm²)</i>
Binary rate multiplier	580	3.75	0.082
Phase detector/integrator	683	20	0.099
Control unit switch, multiplier	500	20	0.069

for the Defense Department's Very High Speed Integrated Circuits Program.

Foundries can produce and package chips as large as 10.7 × 10.7 millimeters. Therefore, using the existing VAX CAD tools and NMOS design rules, one could design and have fabricated a circuit that would contain 30,000 transistors. With the 3 micrometer silicon gate CMOS technology now on line, the existing

Figure 5 — Blowback films at 200X normal chip size are used to verify the final mask artwork. These mask patterns are used to create working plates from which wafers are fabricated. A step-and-repeat process produces working plates with approximately 165 identical copies of these patterns on a 4-inch-diameter circle.

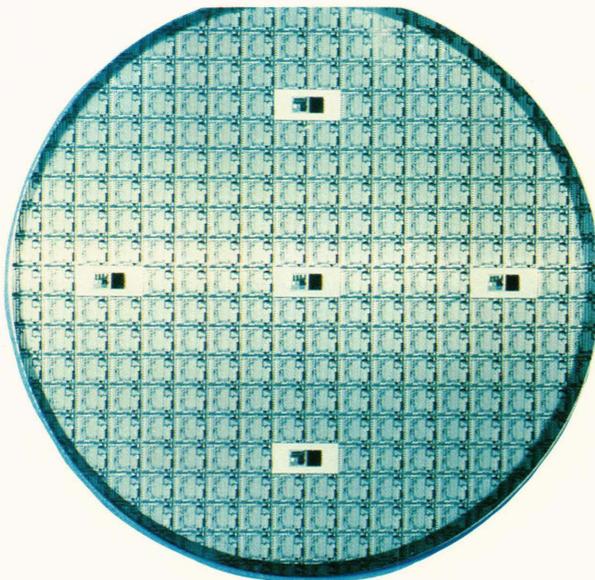
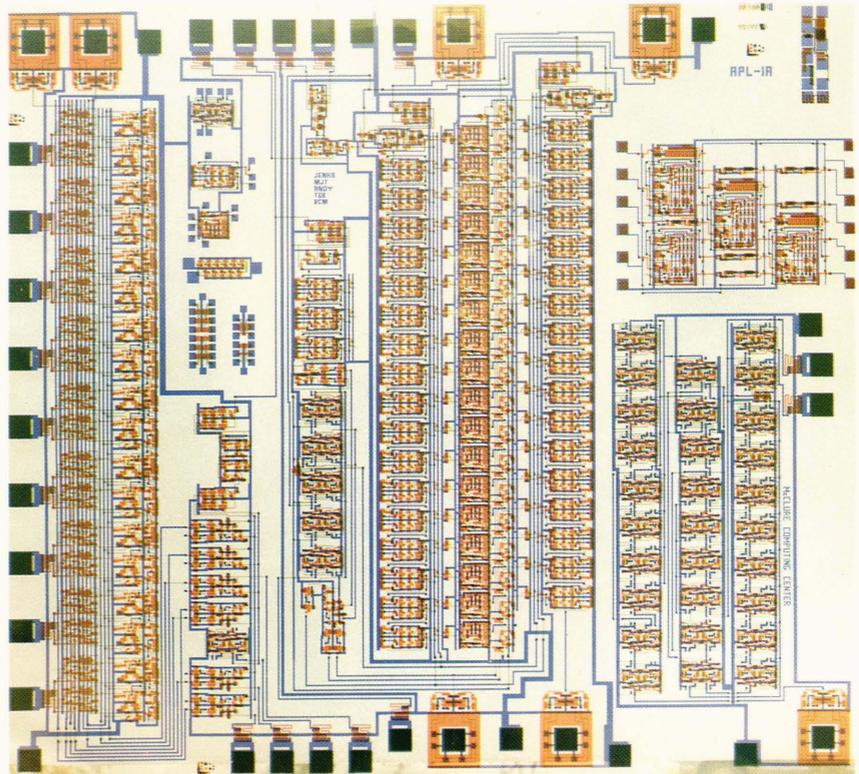


Figure 6 — After processing at a silicon foundry, the completed 4-inch wafer contains approximately 165 potentially good circuits. The five circuits that are different in appearance are called process control monitors. These are standard test circuits used by the silicon foundry to monitor the quality of processing for each wafer. The good wafers are sawed into individual circuits, called chips or dice.

APL facility can design ICs for foundry fabrication with up to 70,000 CMOS transistors, which is true VLSI density. A current project is under way using this CMOS capability to develop a special-purpose

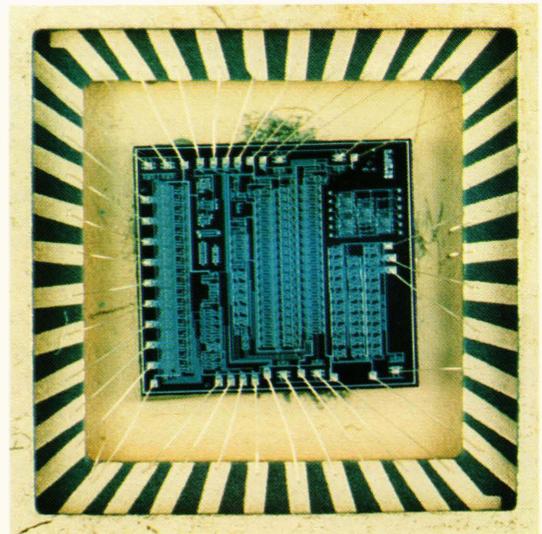


Figure 7 — A die is attached to a suitable package and its pads are wire-bonded to the package pins. Here a 40-pin leadless chip carrier is shown. The die (chip) is 5.00 × 5.56 millimeters; the leadless chip carrier is 12.5 × 12.5 millimeters.

spectrum accumulator chip for use in deep space particle detection experiments.

CONCLUSION

An integrated circuit design capability has been established at APL and has been proven by the creation

of a working custom integrated circuit. The CAD tools used in the facility are adequate for chip designs well into the VLSI level of complexity. The establishment of this facility places APL in a position to take advantage of future improvements in silicon foundry technology for custom VLSI design. Plans to accommodate radiation-hardened CMOS design rules and even gallium arsenide circuits will help keep this phase of activity near the forefront of VLSI technology.

REFERENCE

¹C. A. Mead, "VLSI and Technological Innovation," in *Proc. 1st Caltech Conference on Very Large Scale Integration*, pp. 15-28 (1979).

ACKNOWLEDGMENTS — Several individuals were major contributors to the successful completion of the chip project; among them are A. D. Goldfinger, T. G. Boland, M. J. Thoma, J. E. Penn, and S. E. Deggendorf. The assistance of R. C. Anderson (R. C. Anderson, Inc.) and G. E. Kennedy (Vice President of Comdial Semiconductor, Inc.) is also gratefully acknowledged.